UNIT 3

FIELD EFFECT TRANSISTOR

INTRODUCTION

1. The Field effect transistor is abbreviated as FET , it is an another semiconductor device like a BJT which can be used as an amplifier or switch.
2. The Field effect transistor is a voltage operated device. Whereas Bipolar junction transistor is a current controlled device. Unlike BJT a FET requires virtually no input current.
3. This gives it an extremely high input resistance , which is its most important advantage over a bipolar transistor.
4. FET is also a three terminal device, labeled as source, drain and gate.
5. The source can be viewed as BJT's emitter, the drain as collector, and the gate as the counter part of the base.
6. The material that connects the source to drain is referred to as the channel.
7. FET operation depends only on the flow of majority carriers ,therefore they are called uni polar devices. BJT operation depends on both minority and majority carriers.
8. As FET has conduction through only majority carriers it is less noisy than BJT.
9. FETs are much easier to fabricate and are particularly suitable for ICs because they occupy less space than BJTs.
10. FET amplifiers have low gain bandwidth product due to the junction capacitive effects and produce more signal distortion except for small signal operation.
11. The performance of FET is relatively unaffected by ambient temperature changes. As it has a negative temperature coefficient at high current levels, it prevents the FET from thermal breakdown. The BJT has a positive temperature coefficient at high current levels which leads to thermal breakdown.

CLASSIFICATION OF FET:

There are two major categories of field effect transistors:

1. Junction Field Effect Transistors

2. MOSFETs

These are further sub divided in to P- channel and N-channel devices.

MOSFETs are further classified in to two types Depletion MOSFETs and Enhancement . MOSFETs

When the channel is of N-type the JFET is referred to as an N-channel JFET ,when the channel is of P-type the JFET is referred to as P-channel JFET.

The schematic symbols for the P-channel and N-channel JFETs are shown in the figure.

Fig 5.1 schematic symbols for the P-channel and N-channel JFET

CONSTRUCTION AND OPERATION OF N- CHANNEL FET

If the gate is an N-type material, the channel must be a P-type material.

CONSTRUCTION OF N-CHANNEL JFET

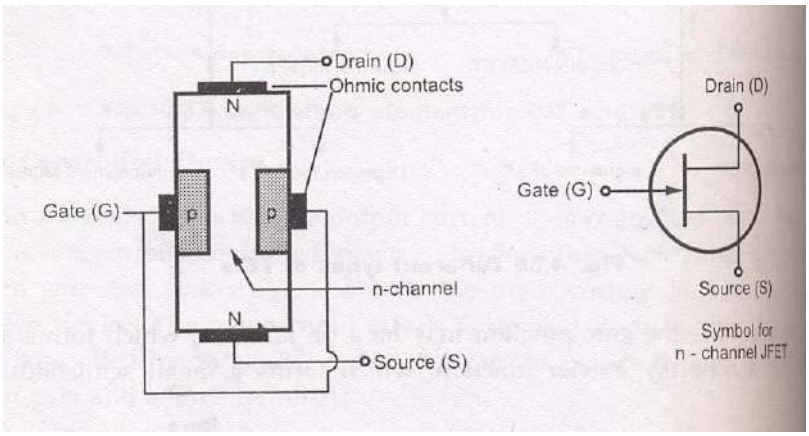


Fig 5.2 Construction of N-Channel JFET

A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source. And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

OPERATION OF N-CHANNEL JFET:-

The overall operation of the JFET is based on varying the width of the channel to control the drain current.

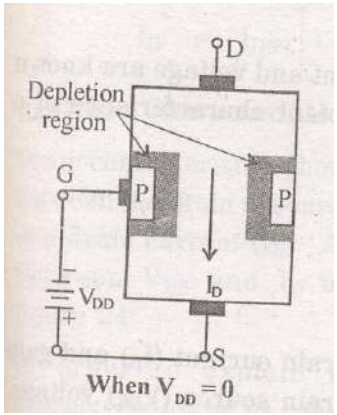
A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate. With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed. The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut off completely.

There are two ways to control the channel width

1. By varying the value of Vgs
2. And by Varying the value of Vds holding Vgs constant

1 By varying the value of Vgs :-

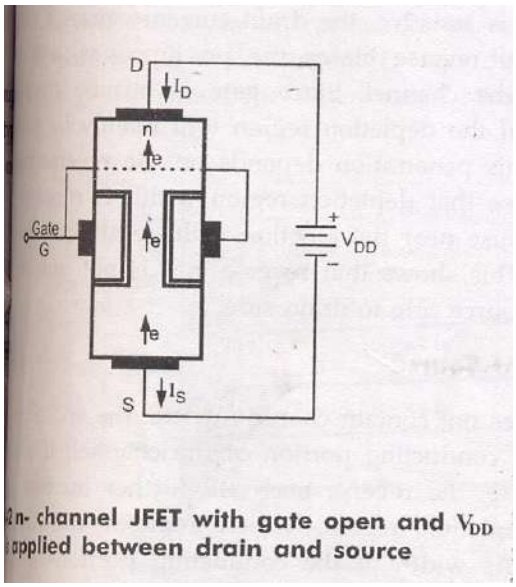
We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a battery voltage Vgs connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



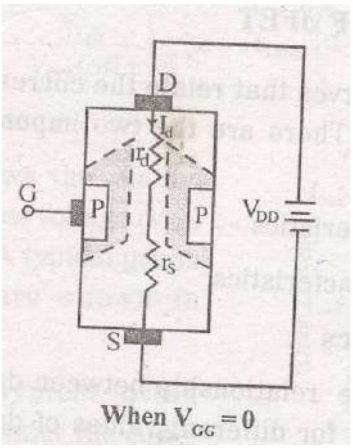
1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides , the region containing these immobile ions is known as depletion regions.
2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.
3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.
4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction.
5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases .
6) By varying the value of Vgs we can vary the width of the channel.

2 Varying the value of Vds holding Vgs constant :-

1) When no voltage is applied to the gate i.e. Vgs=0 , Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current Id .
2) With Vgs= 0 for Id= 0 the channel between the gate junctions is entirely open .In response to a small applied voltage Vds , the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds .
3) The channel resistances are represented as rd and rs as shown in the fig.



n- channel JFET with gate open and V_{DD} applied between drain and source



When $V_{GG} = 0$

4) This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction,(rd> rs) .Thus the depletion region is formed which is not symmetrical .

5) The depletion region i.e. developed penetrates deeper in to the channel near drain and less towards source because Vrd >> Vrs. So reverse bias is higher near drain than at source.
6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off. This is the voltage where the current Id begins to level off and approach a constant value.
7) So, by varying the value of Vds we can vary the width of the channel holding Vgs constant.

When both Vgs and Vds is applied:-

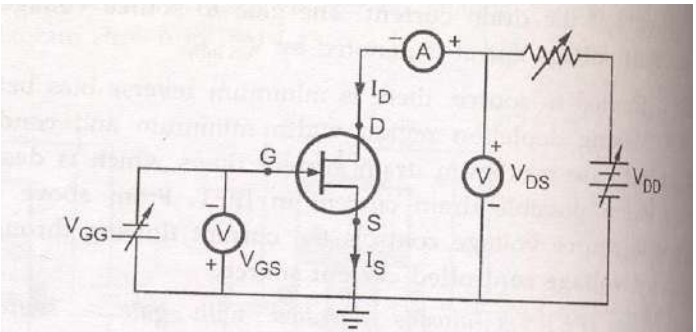
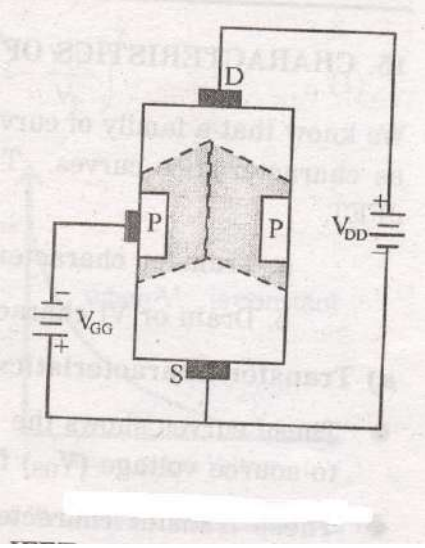


Fig. 4.45 Experimental setup to plot JFET characteristics

It is of course in principle not possible for the channel to close Completely and there by reduce the current Id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

1) When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current Id, its conventional direction is from drain to source.
2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by Idss.



3) When Vgs is increased beyond Zero the depletion regions are widened. This reduces the effective width of the channel and therefore controls the flow of drain current through the channel.
4) When Vgs is further increased a stage is reached at which to depletion regions touch each other that means the entire channel is closed with depletion region. This reduces the drain current to Zero.

CHARACTERISTICS OF N-CHANNEL JFET

The family of curves that shows the relation between current and voltage are known as characteristic curves.

There are two important characteristics of a JFET.

1) Drain or VI Characteristics
2) Transfer characteristics

1. Drain Characteristics:-

Drain characteristics shows the relation between the drain to source voltage Vds and drain current Id. In order to explain typical drain characteristics let us consider the curve with Vgs= 0.V.

1) When Vds is applied and it is increasing the drain current ID also increases linearly up to knee point.
2) This shows that FET behaves like an ordinary resistor.This region is called as ohmic region.
3) ID increases with increase in drain to source voltage. Here the drain current is increased slowly as compared to ohmic region.

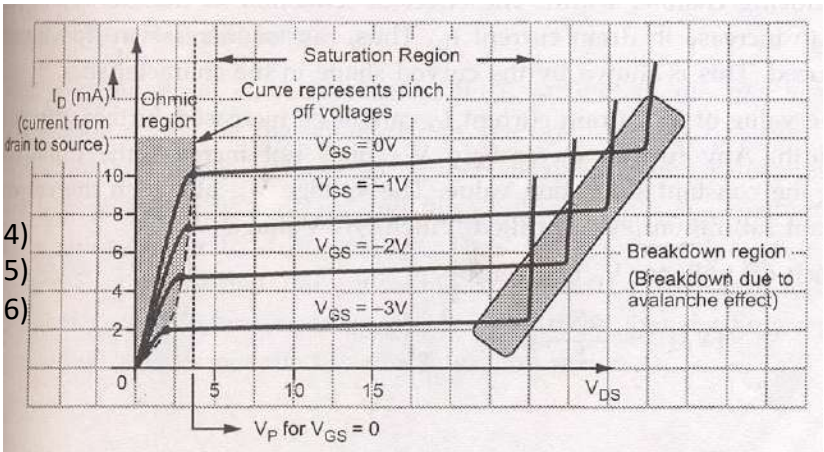


Fig. 4.44 Drain V-I characteristics of n-channel JFET

4)
5)
6)

4) It is because of the fact that there is an increase in VDS .This in turn increases the reverse bias voltage across the gate source junction .As a result of this depletion region grows in size thereby reducing the effective width of the channel.

5) All the drain to source voltage corresponding to point the channel width is reduced to a minimum value and is known as pinch off.

5) The drain to source voltage at which channel pinch off occurs is called pinch off voltage(Vp).

PINCH OFF Region:-

1) This is the region shown by the curve as saturation region.
2) It is also called as saturation region or constant current region. Because of the channel is occupied with depletion region , the depletion region is more towards the drain and less towards the source, so the channel is limited, with this only limited number of carriers are only allowed to cross this channel from source drain causing a current that is constant in this region. To use FET as an amplifier it is operated in this saturation region.
3) In this drain current remains constant at its maximum value IDSS.

4) The drain current in the pinch off region depends upon the gate to source voltage and is given by the relation

$$I_d = I_{dss} [1 - V_{gs/Vp}]^2$$

This is known as shokley's relation.

BREAKDOWN REGION:-

1) The region is shown by the curve .In this region, the drain current increases rapidly as the drain to source voltage is increased.
2) It is because of the gate to source junction due to avalanche effect.

3) The avalanche break down occurs at progressively lower value of VDS because the reverse bias gate voltage adds to the drain voltage thereby increasing effective voltage across the gate junction
This causes

1. The maximum saturation drain current is smaller
2. The ohmic region portion decreased.

4) It is important to note that the maximum voltage VDS which can be applied to FET is the lowest voltage which causes available break down.

2. TRANSFER CHARACTERISTICS:-

These curves shows the relationship between drain current ID and gate to source voltage VGS for different values of VDS.

1) First adjust the drain to source voltage to some suitable value , then increase the gate to source voltage in small suitable value.
2) Plot the graph between gate to source voltage along the horizontal axis and current ID on the vertical axis. We shall obtain a curve like this.

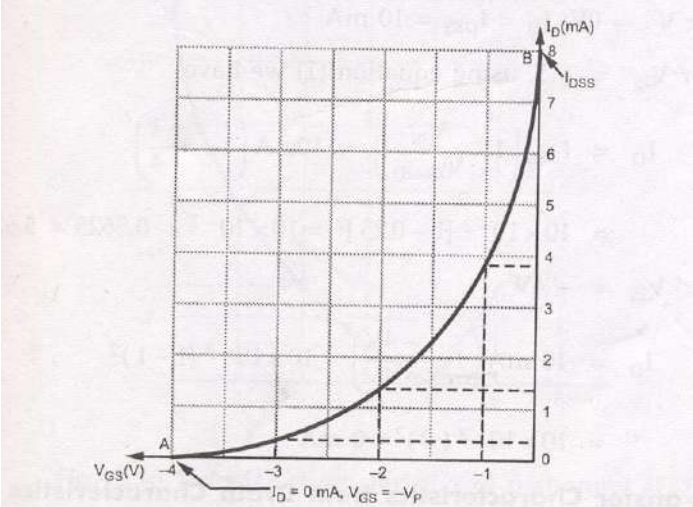


Fig. 4.48 Transfer characteristics of n-channel JFET

3) As we know that if V_{gs} is more negative curves drain current to reduce . where V_{gs} is made sufficiently negative, I_d is reduced to zero. This is caused by the widening of the depletion region to a point where it is completely closes the channel. The value of V_{gs} at the cutoff point is designed as V_{gsoff}

4) The upper end of the curve as shown by the drain current value is equal to I_{dss} that is when $V_{gs} = 0$ the drain current is maximum.

5) While the lower end is indicated by a voltage equal to V_{gsoff}
6) If Vg_s continuously increasing , the channel width is reduced , then $I_d = 0$
7) It may be noted that curve is part of the parabola; it may be expressedas

$I_d = I_{dss}[1 - V_{gs}/V_{gsoff}]^2$

DIFFERENCE BETWEEN V_p AND V_{gsoff} –

Vp is the value of V_{gs} that causes the JFET to become constant current component, It is measured at $V_{gs} = 0V$ and has a constant drain current of $I_d = I_{dss}$ .Where V_{gsoff} is the value of V_{gs} that reduces I_d to approximately zero.

Why the gate to source junction of a JFET be always reverse biased ?

The gate to source junction of a JFET is never allowed to become forward biased because the gate material is not designed to handle any significant amount of current. If the junction is allowed to become forward biased, current is generated through the gate material. This current may destroy the component.

There is one more important characteristic of JFET reverse biasing i.e. J FET 's have extremely high characteristic gate input impedance. This impedance is typically in the high mega ohm range. With the advantage of extremely high input impedance it draws no current from the source. The high input impedance of the JFET has led to its extensive use in integrated circuits. The low current requirements of the component makes it perfect for use in ICs. Where thousands of transistors must be etched on to a single piece of silicon. The low current draw helps the IC to remain relatively cool, thus allowing more components to be placed in a smaller physical area.

JFET PARAMETERS

The electrical behavior of JFET may be described in terms of certain parameters. Such parameters are obtained from the characteristic curves.

A C Drain resistance(r_d):

It is also called dynamic drain resistance and is the a.c.resistance between the drain and source terminal,when the JFET is operating in the pinch off or saturation region.It is given by the ratio of small change in drain to source voltage ΔV_{ds} to the corresponding change in drain current ΔI_d for a constant gate to source voltage V_{gs}.

Mathematically it is expressed as $r_d = \Delta V_{ds} / \Delta I_d$ where V_{gs} is held constant.

TRANCE CONDUCTANCE (g_m):

It is also called forward transconductance . It is given by the ratio of small change in drain current (ΔI_d) to the corresponding change in gate to source voltage (ΔV_{ds})

Mathematically the transconductance can be written as

$$g_m=\Delta I_{d/}\Delta V_{ds}$$

AMPLIFICATION FACTOR (μ)

It is given by the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs})for a constant drain current (I_d).

Thus $\mu=\Delta V_{ds}/\Delta V_{gs}$ when I_d held constant

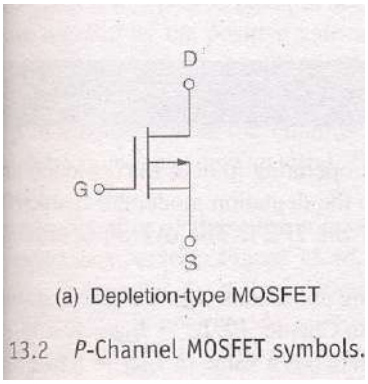
The amplification factor μ may be expressed as a product of transconductance (g_m)and ac drain resistance (r_d)

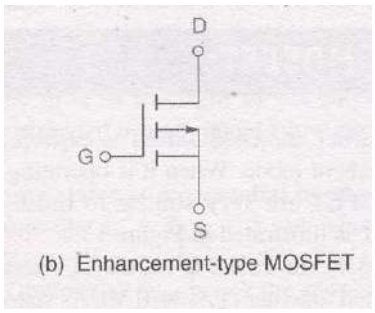
$\mu=\Delta V_{ds}/\Delta V_{gs}=g_m r_d$

MOSFET

We now turn our attention to the insulated gate FET or metal oxide semi conductor FET which is having the greater commercial importance than the junction FET.

Most MOSFETS however are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.





(a) Depletion type MOSFET (b) Enhancement type MOSFET

Both of them are P- channel

Here are two basic types of MOSFETS

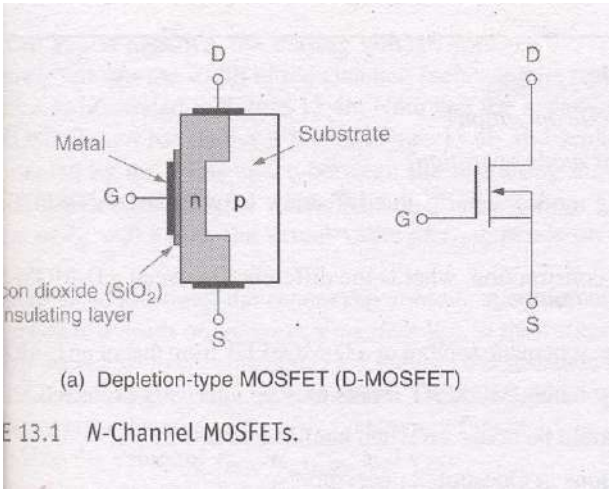
(1) Depletion type (2) Enhancement type MOSFET.

MOSFETS can be operated in both the depletion mode and the enhancement mode.

E -MOSFETS

are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

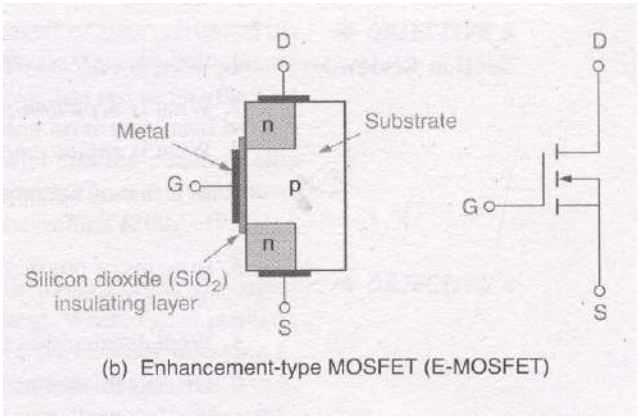
The construction difference between the two is shown in the fig given below.



(a) Depletion-type MOSFET (D-MOSFET)

E 13.1 *N*-Channel MOSFETs.

As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



(b) Enhancement-type MOSFET (E-MOSFET)

The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals.

Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SIO_2 a glass like insulating material. The gate material is made up of

metal conductor .Thus going from gate to substrate, we can have metal oxide semi conductor which is where the term MOSFET comes from.

Since the gate is insulated from the rest of the component, the MOSFET is sometimes referred to as an insulated gate FET or IGFET.

The foundation of the MOSFET is called the substrate. This material is represented in the schematic symbol by the center line that is connected to the source.

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing in represents an N-channel device, while an arrow pointing out represents p-channel device.

CONSTRUCTION OF AN N-CHANNEL MOSFET:-

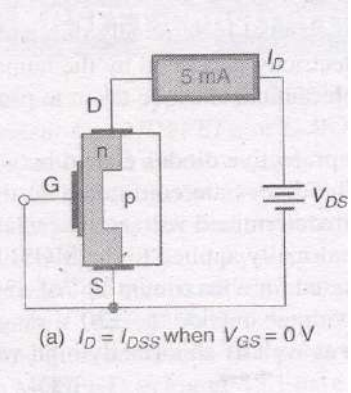
The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections , which will act as source and drain.

A thin layer of insulation silicon dioxide (SIO_2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region.Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of sio2

Is the reason why this device is called the insulated gate field effect transistor. This layer results in an extremely high input resistance (10 10 to 10power 15ohms) for MOSFET.

DEPLETION MOSFET

The basic structure of D –MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current IDSS flows foe zero gate to source voltage, Vgs=0.



Depletion mode operation:-

1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together(VGS=0V)

2) At this stage ID= IDSS where VGS=0V, with this voltage VDS, an appreciable drain current IDSS flows.

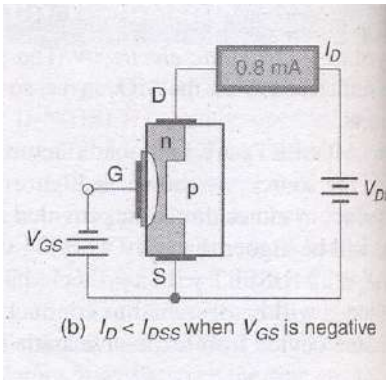
3) If the gate to source voltage is made negative i.e. VGs is negative .Positive charges are induced in the channel through the SIO2 of the gate capacitor.

4) Since the current in a FET is due to majority carriers(electrons for an N-type material) , the induced positive charges make the channel less conductive and the drain current drops as Vgsis made more negative.

5) The re distribution of charge in the channel causes an effective depletion of majority carriers , which accounts for the designation depletion MOSFET.

6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel , increasing its resistance.

7) Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.



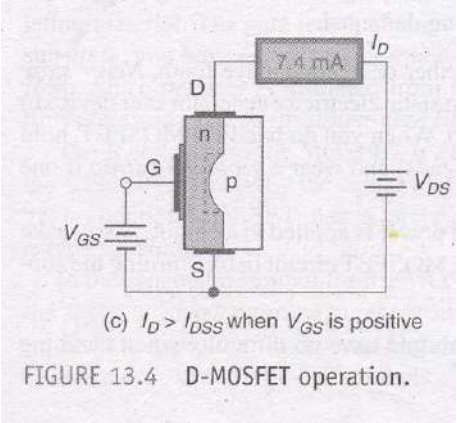
(b) $I_D < I_{DSS}$ when V_{GS} is negative

8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result ,Id<Idss.The actual value of ID depends on the value of Idss,Vgs(off) and Vgs.

<u>Enhancement mode operation of the D-MOSFET:-</u>

1) This operating mode is a result of applying a positive gate to source voltage Vgs to thedevice.
2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of IDSS
3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.

4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the +gate voltage.
5) With the build up of electrons near the channel , the area to the right of the physical channel effectively becomes an N type material.
6) The extended n type channel now allows more current, Id> Idss



(c) $I_D > I_{DSS}$ when V_{GS} is positive

FIGURE 13.4 D-MOSFET operation.

Characteristics of Depletion MOSFET:-

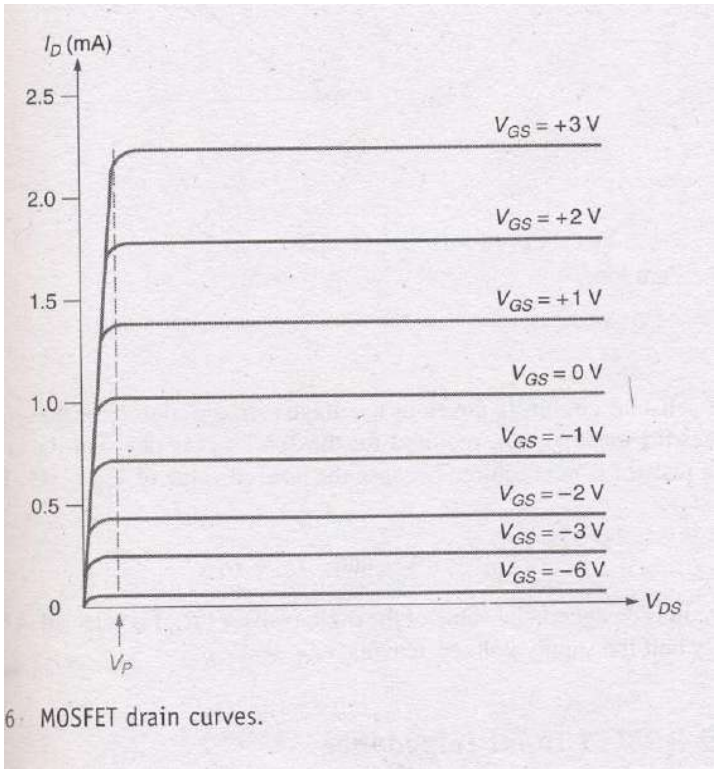
The fig. shows the drain characteristics for the N channel depletion type MOSFET

1) The curves are plotted for both Vgs positive and Vgs negative voltages
.
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive,the MOSFET operates in the enhancement mode.
3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of Vgs.

4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increases linearly.

5) But as Vgs,0 induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. Id is constant.

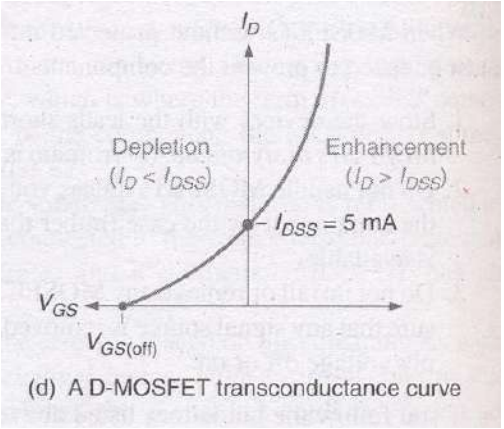
6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source. again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Fig



6 MOSFET drain curves.

TRANSFER CHARACTERISTICS:-

The combination of 3 operating states i.e. Vgs=0V, VGs<0V, Vgs>0V is represented by the D MOSFET transconductance curve shown in Fig.



(d) A D-MOSFET transconductance curve

1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET.

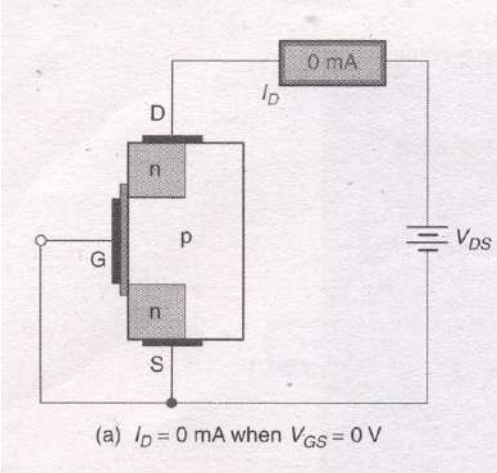
2) This curve extends for the positive values of Vgs

3) Note that Id=Idss for Vgs=0V when Vgs is negative,Id< Idss when Vgs= Vgs(off) ,Id is reduced to approximately omA.Where Vgs is positive Id>Idss.So obviously Idss is not the maximum possible value of Id for a MOSFET.

4) The curves are similar to JFET so thet the D MOSFET have the same transconductance equation.

E-MOSFETS:-

The E MOSFET is capable of operating only in the enhancement mode.The gate potential must be positive w.r.t to source.



(a) $I_D = 0$ mA when $V_{GS} = 0$ V

1) when the value of Vgs=0V, there is no channel connecting the source and drain materials.

2) As aresult , there can be no significant amount of drain current.

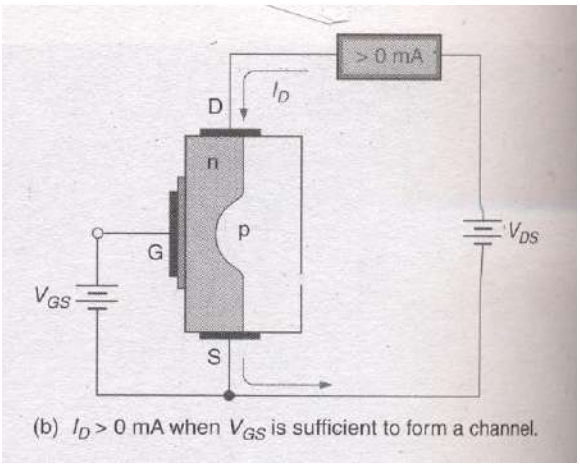
3) When Vgs=0, the Vdd supply tries to force free electrons from source to drain but the presence of p-region does not permit the electrons to pass through it. Thus there is no drain current at Vgs=0,

4) If Vgs is positive, it induces a negative charge in the p type substrate just adjacent to the SIO2 layer.

5) As the holes are repelled by the positive gate voltage, the minority carrier electrons attracted toward this voltage. This forms an effective N type bridge between source and drain providinga path for drain current.

6) This +ve gate voltage forma a channel between the source and drain.

7) This produces a thin layer of N type channel in the P type substarate.This layer of free electrons is called N type inversion layer.



(b) $I_D > 0$ mA when V_{GS} is sufficient to form a channel.

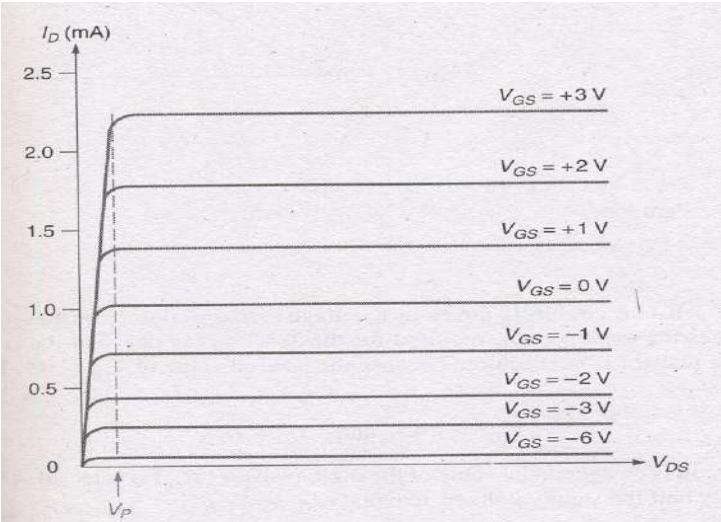
8) The minimum Vgs which produces this inversion layer is called threshold voltage and is designated by Vgs(th).This is the point at which the device turns on is called the threshold voltage Vgs(th)
9) When the voltage Vgs is <Vgs (th) no current flows from drain to source.

10) How ever when the voltage Vgs > Vgs (th) the inversion layer connects the drain to source and we get significant values of current.

CHARACTERISTICS OF E- MOSFET:-

1. **DRAIN CHARACTERISTICS**

The volt ampere drain characteristics of an N-channel enhancement mode MOSFET are given in the fig.



6 MOSFET drain curves.

2. TRANSFER CHARACTERISTICS:-

1) The current Idss at Vgs≤ 0 is very small beinf of the order of a few nano amps.
2) As Vgs is made +ve , the current Id increases slowly at forst, and then much more rapidly with an increase in Vgs.
3) The standard transconductance formula will not work for the E MOSFET.
4) To determine the value of ID at a given value of VGs we must use the following relation

$$Id = K[V_{gs} - V_{gs(Th)}]^2$$

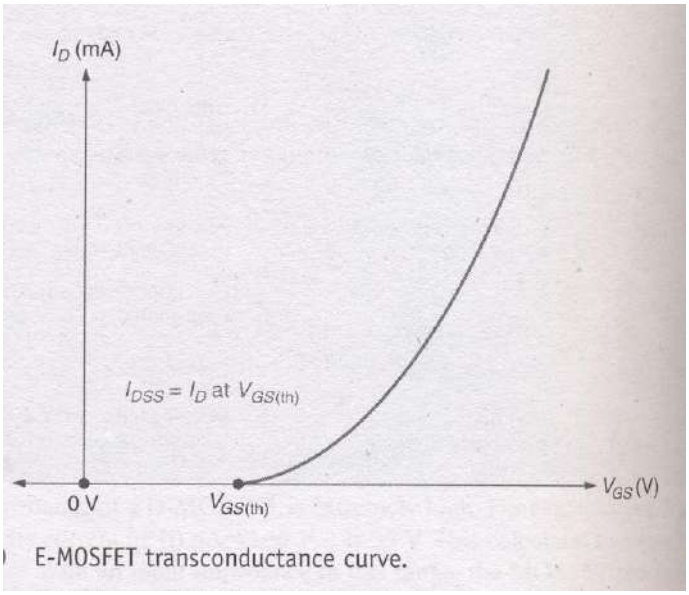
Where K is constant for the MOSFET . found as

$$K = \frac{Id(on)}{[vgs(on) - Vgs(Th)]2}$$

From the data specification sheets, the 2N7000 has the following ratings.

Id(on)= 75mA(minimum).

And Vgs(th)=0.8(minimum)



E-MOSFET transconductance curve.

APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETs can be found in the area of digital (computer electronics). The signals in digital circuits are made up of rapidly switching dc levels. This signal is called as a rectangular wave ,made up of two dc levels (or logic levels). These logic levels are 0V and +5V.

A group of circuits with similar circuitry and operating characteristics is referred to as a logic family. All the circuits in a given logic family respond to the same logic levels, have similar speed and power-handling capabilities , and can be directly connected together. One such logic family is complementary MOS (or CMOS) logic. This logic family is made up entirely of MOSFETs.

UNIT-4

Feedback Amplifier & Oscillator

Feedback Amplifier

A practical amplifier has a gain of nearly one million *i.e.* its output is one million times the input. Consequently, even a casual disturbance at the input will appear in the amplified form in the output. There is a strong tendency in amplifiers to introduce *hum* due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output. The noise in the output of an amplifier is undesirable and must be kept to as small a level as possible. The noise level in amplifiers can be reduced considerably by the use of *negative feedback i.e*. by injecting a fraction of output in phase opposition to the input signal. The object of this chapter is to consider the effects and methods of providing negative feedback in transistor amplifiers.

Ideally an amplifier should reproduce the input signal, with change in magnitude and with or without change in phase. But some of the short comings of the amplifier circuit are

1. Change in the value of the gain due to variation in supplying voltage, temperature or due to components.
2. Distortion in wave-form due to non linearities in the operating characters of the Amplifying device.
3. The amplifier may introduce noise (undesired signals)

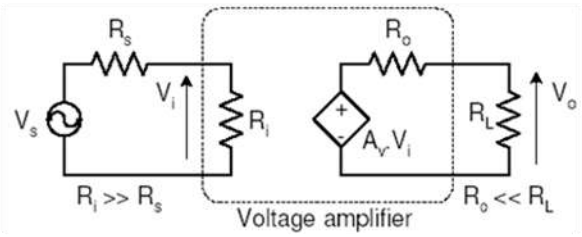
The above drawbacks can be minimizing if we introduce feedback.

CLASSIFICATION OF AMPLIFIERS

Amplifiers can be classified broadly as:

1. Voltage amplifiers.
2. Current amplifiers.
3. Tran conductance amplifiers.
4. Tran resistance amplifiers.

1.1 Voltage amplifier



if $R_i >> R_s$

then $V_i \approx V_s$

and if $R_o << R_L$

then

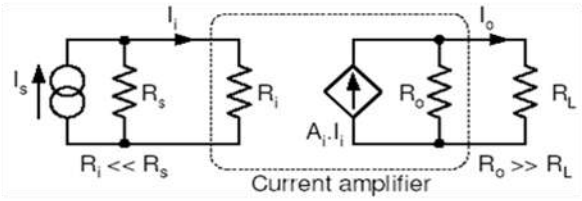
$$V_o \approx A_v V_i \approx A_v V_s$$

hence $A_v \equiv \frac{V_o}{V_i}$

with $R_L = \infty$

represent the open circuit voltage gain.

1.2 Current amplifier



if $R_i << R_s$

then $I_i \approx I_s$

and if $R_o >> R_L$

then

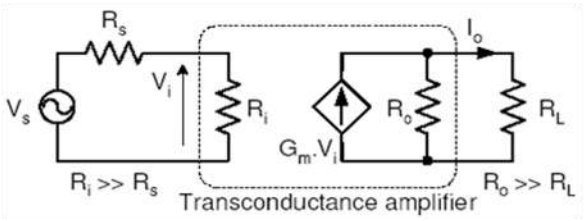
$$I_o \approx A_i I_i \approx A_i I_s$$

hence $A_i \equiv \frac{I_o}{I_i}$

with $R_L = 0$

represent the short circuit current gain.

1.3 Transconductance amplifier



if $R_i >> R_s$

then $V_i \approx V_s$

and if $R_o >> R_L$

then

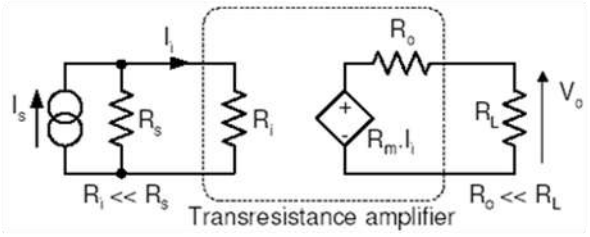
$$I_o \approx G_m V_i \approx G_m V_s$$

hence $G_m \equiv \frac{I_o}{V_i}$

with $R_L = 0$

represent the short circuit mutual or transfer conductance

1.4 Transresistance amplifier



if $R_i << R_s$

then $I_i \approx I_s$

and if $R_o << R_L$

then

$$V_o \approx R_m I_i \approx R_m i_s$$

hence $R_m \equiv \frac{V_o}{I_i}$

with $R_L = \infty$

represent the open circuit mutual or transfer resistance.

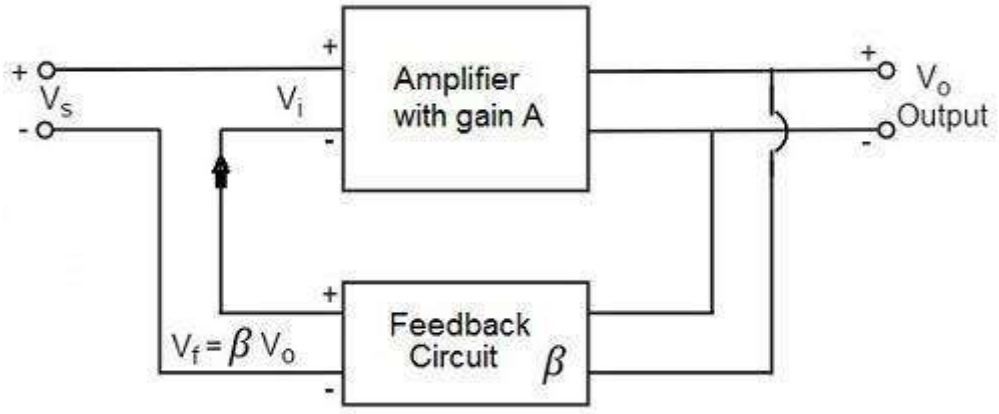
Concept of Feedback

An amplifier circuit simply increases the signal strength. But while amplifying, it just increases the strength of its input signal whether it contains information or some noise along with information. This noise or some disturbance is introduced in the amplifiers because of their strong tendency to introduce hum due to sudden temperature changes or stray electric and magnetic fields. Therefore, every high gain amplifier tends to give noise along with signal in its output, which is very undesirable.

The noise level in the amplifier circuits can be considerably reduced by using negative feedback done by injecting a fraction of output in phase opposition to the input signal.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are theamplifier and the feedback circuit. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure.



From the above figure, the gain of the amplifier is represented as A. the gain of the amplifier is the ratio of output voltage V_o to the input voltage V_i. the feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s. Now,

$Vi=Vs+Vf=Vs+\beta Vo$
$Vi=Vs-Vf=Vs-\beta Vo$

The quantity $\beta = V_f/V_o$ is called as feedback ratio or feedback fraction.

Let us consider the case of negative feedback. The output $V_o$must be equal to the input voltage ($V_s - \beta V_o$) multiplied by the gain A of the amplifier.

Hence,

$$(V_s - \beta V_o)A = V_o$$

Or

$$AV_s - A\beta V_o = V_o$$

Or

$$AV_s = V_o(1 + A\beta)$$

Therefore,

$$\frac{Vo}{Vs} = \frac{A}{1 + A\beta}$$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s, i.e.,

$$Af = \frac{A}{1 + A\beta}$$

The equation of gain of the feedback amplifier, with positive feedback is given by

$$Af = \frac{A}{1 - A\beta}$$

These are the standard equations to calculate the gain of feedback amplifiers.

Types of Feedbacks

The process of injecting a fraction of output energy of some device back to the input is known as Feedback. It has been found that feedback is very useful in reducing noise and making the amplifier operation stable.

Depending upon whether the feedback signal aids or opposes the input signal, there are two types of feedbacks used.

Positive Feedback

The feedback in which the feedback energy i.e., either voltage or current is in phase with the input signal and thus aids it is called asPositive feedback.

Both the input signal and feedback signal introduces a phase shift of 180^o thus making a 360^o resultant phase shift around the loop, to be finally in phase with the input signal.

Though the positive feedback increases the gain of the amplifier, it has the disadvantages such as

- Increasing distortion
- Instability

It is because of these disadvantages the positive feedback is not recommended for the amplifiers. If the positive feedback is sufficiently large, it leads to oscillations, by which oscillator circuits are formed.

Negative Feedback

The feedback in which the feedback energy i.e., either voltage or current is out of phase with the input and thus opposes it, is called as negative feedback.

In negative feedback, the amplifier introduces a phase shift of 180^o into the circuit while the feedback network is so designed that it produces no phase shift or zero phase shift. Thus the resultant feedback voltage V_f is 180^o out of phase with the input signal V_{in}.

Though the gain of negative feedback amplifier is reduced, there are many advantages of negative feedback such as

- Stability of gain is improved
- Reduction in distortion
- Reduction in noise
- Increase in input impedance
- Decrease in output impedance
- Increase in the range of uniform application

It is because of these advantages negative feedback is frequently employed in amplifiers.

Negative feedback in an amplifier is the method of feeding a portion of the amplified output to the input but in opposite phase. The phase opposition occurs as the amplifier provides 180^o phase shift whereas the feedback network doesn't.

While the output energy is being applied to the input, for the voltage energy to be taken as feedback, the output is taken in shunt connection and for the current energy to be taken as feedback, the output is taken in series connection.

There are two main types of negative feedback circuits. They are −

- Negative Voltage Feedback
- Negative Current Feedback

Negative Voltage Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output voltage. This is further classified into two types −

- Voltage-series feedback
- Voltage-shunt feedback

Negative Current Feedback

In this method, the voltage feedback to the input of amplifier is proportional to the output current. This is further classified into two types.

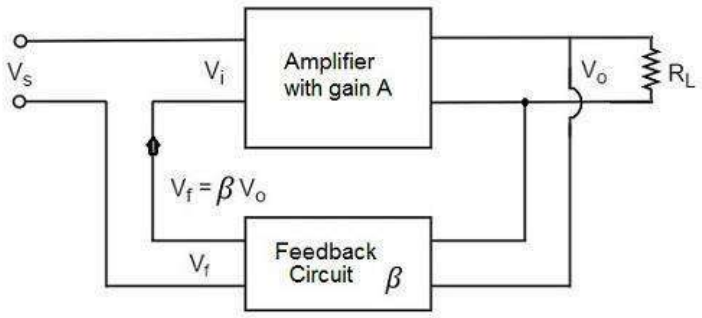
- Current-series feedback
- Current-shunt feedback

Let us have a brief idea on all of them.

Voltage-Series Feedback

In the voltage series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as shunt-driven series-fed feedback, i.e., a parallel-series circuit.

The following figure shows the block diagram of voltage series feedback, by which it is evident that the feedback circuit is placed in shunt with the output but in series with the input.

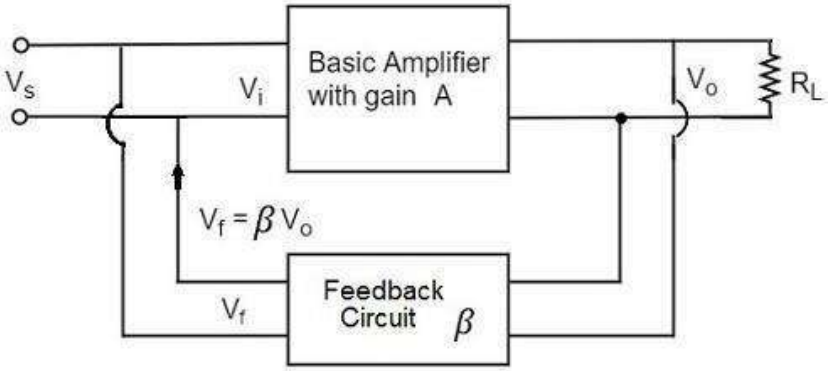


As the feedback circuit is connected in shunt with the output, the output impedance is decreased and due to the series connection with the input, the input impedance is increased.

Voltage-Shunt Feedback

In the voltage shunt feedback circuit, a fraction of the output voltage is applied in parallel with the input voltage through the feedback network. This is also known as shunt-driven shunt-fed feedback i.e., a parallel-parallel proto type.

The below figure shows the block diagram of voltage shunt feedback, by which it is evident that the feedback circuit is placed in shunt with the output and also with the input.

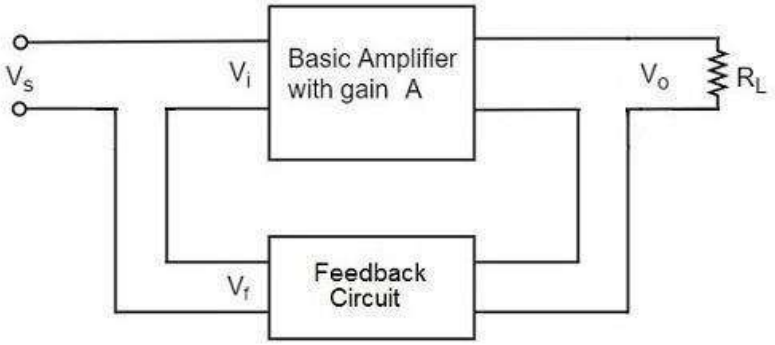


As the feedback circuit is connected in shunt with the output and the input as well, both the output impedance and the input impedance are decreased.

Current-Series Feedback

In the current series feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as series-driven series-fed feedback i.e., a series-series circuit.

The following figure shows the block diagram of current series feedback, by which it is evident that the feedback circuit is placed in series with the output and also with the input.

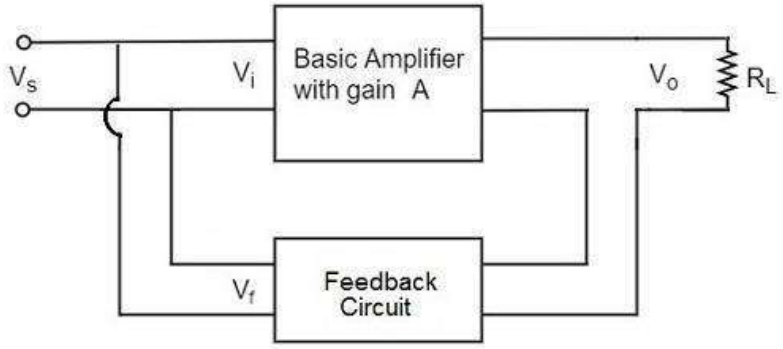


As the feedback circuit is connected in series with the output and the input as well, both the output impedance and the input impedance are increased.

Current-Shunt Feedback

In the current shunt feedback circuit, a fraction of the output voltage is applied in series with the input voltage through the feedback circuit. This is also known as series-driven shunt-fed feedback i.e., a series-parallel circuit.

The below figure shows the block diagram of current shunt feedback, by which it is evident that the feedback circuit is placed in series with the output but in parallel with the input.



As the feedback circuit is connected in series with the output, the output impedance is increased and due to the parallel connection with the input, the input impedance is decreased.

Let us now tabulate the amplifier characteristics that get affected by different types of negative feedbacks.

Characteristics	**Types of Feedback**			
	Voltage-Series	**Voltage-Shunt**	**Current-Series**	**Current-Shunt**
Voltage Gain	Decreases	Decreases	Decreases	Decreases
Bandwidth	Increases	Increases	Increases	Increases
Input resistance	Increases	Decreases	Increases	Decreases
Output resistance	Decreases	Decreases	Increases	Increases
Harmonic distortion	Decreases	Decreases	Decreases	Decreases
Noise	Decreases	Decreases	Decreases	Decreases

Advantages of Negative Feedback

1. Stabilization of gain
   - Make the gain less sensitive to changes in circuit components e.g. due to changes in temperature.
2. Reduce non-linear distortion
   - Make the output proportional to the input, keeping the gain constant, independent of signal level.
3. Reduce the effect of noise
   - Minimize the contribution to the output of unwanted signals generated in circuit components or extraneous interference.
4. Extend the bandwidth of the amplifier
   - Reduce the gain and increase the bandwidth
5. Modification the input and output impedances
   - Raise or lower the input and output impedances by selection of the appropriate feedback topology.

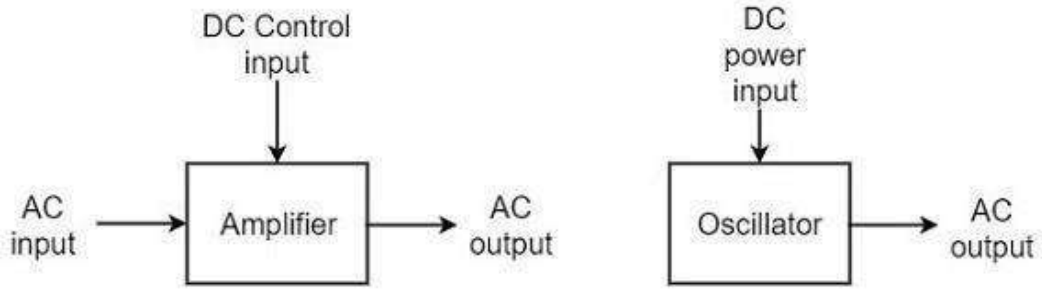
Oscillators

An **oscillator** generates output without any ac input signal. An electronic oscillator is a circuit which converts dc energy into ac at a very high frequency. An amplifier with a positive feedback can be understood as an oscillator.

Amplifier vs. Oscillator

An **amplifier** increases the signal strength of the input signal applied, whereas an **oscillator** generates a signal without that input signal, but it requires dc for its operation. This is the main difference between an amplifier and an oscillator.

Take a look at the following illustration. It clearly shows how an amplifier takes energy from d.c. power source and converts it into a.c. energy at signal frequency. An oscillator produces an oscillating a.c. signal on its own.



The frequency, waveform, and magnitude of a.c. power generated by an amplifier, is controlled by the a.c. signal voltage applied at the input, whereas those for an oscillator are controlled by the components in the circuit itself, which means no external controlling voltage is required.

Alternator vs. Oscillator

An **alternator** is a mechanical device that produces sinusoidal waves without any input. This a.c. generating machine is used to generate frequencies up to 1000Hz. The output frequency depends on the number of poles and the speed of rotation of the armature.

The following points highlight the differences between an alternator and an oscillator −

- An alternator converts mechanical energy to a.c. energy, whereas the oscillator converts d.c. energy into a.c. energy.
- An oscillator can produce higher frequencies of several MHz whereas an alternator cannot.
- An alternator has rotating parts, whereas an electronic oscillator doesn't.
- It is easy to change the frequency of oscillations in an oscillator than in an alternator.

Oscillators can also be considered as opposite to rectifiers that convert a.c. to d.c. as these convert d.c. to a.c.

Classification of Oscillators

Electronic oscillators are classified mainly into the following two categories −

- **Sinusoidal Oscillators** − The oscillators that produce an output having a sine waveform are called **sinusoidal** or **harmonic oscillators**. Such oscillators can provide output at frequencies ranging from 20 Hz to 1 GHz.
- **Non-sinusoidal Oscillators** − The oscillators that produce an output having a square, rectangular or saw-tooth waveform are called **non-sinusoidal** or **relaxation oscillators**. Such oscillators can provide output at frequencies ranging from 0 Hz to 20 MHz.

Sinusoidal Oscillators

Sinusoidal oscillators can be classified in the following categories −

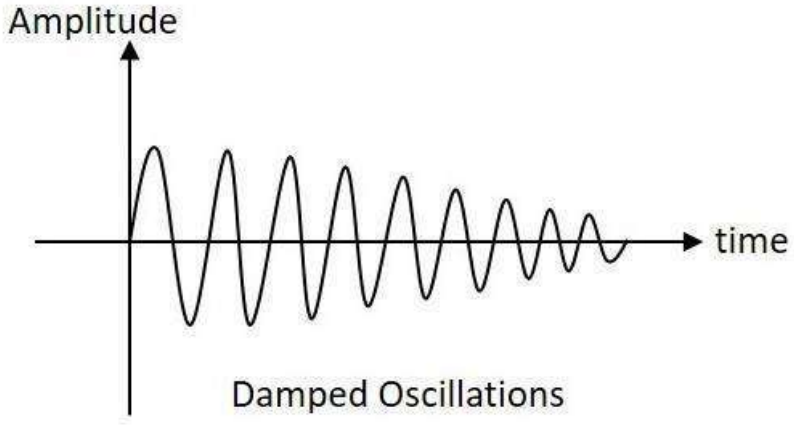
- **Tuned Circuit Oscillators** − These oscillators use a tuned-circuit consisting of inductors (L) and capacitors (C) and are used to generate high-frequency signals. Thus they are also known as radio frequency R.F. oscillators. Such oscillators are Hartley, Colpitts, Clapp-oscillators etc.
- **RC Oscillators** − There oscillators use resistors and capacitors and are used to generate low or audio-frequency signals. Thus they are also known as audio-frequency (A.F.) oscillators. Such oscillators are Phase –shift and Wein-bridge oscillators.
- **Crystal Oscillators** − These oscillators use quartz crystals and are used to generate highly stabilized output signal with frequencies up to 10 MHz. The Piezo oscillator is an example of a crystal oscillator.
- **Negative-resistance Oscillator** − These oscillators use negative-resistance characteristic of the devices such as tunnel devices. A tuned diode oscillator is an example of a negative-resistance oscillator.

Nature of Sinusoidal Oscillations

The nature of oscillations in a sinusoidal wave is generally of two types. They are **damped** and **undamped oscillations**.

Damped Oscillations

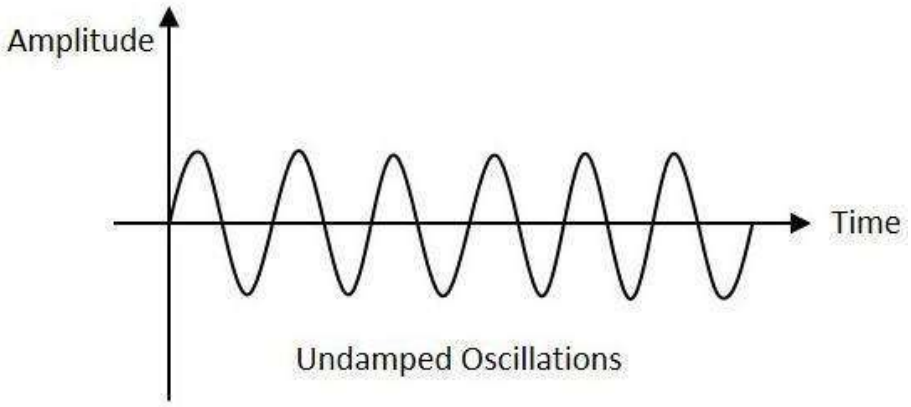
The electrical oscillations whose amplitude goes on decreasing with time are called as **Damped Oscillations**. The frequency of the damped oscillations may remain constant depending upon the circuit parameters.



Damped oscillations are generally produced by the oscillatory circuits that produce power losses and doesn't compensate if required.

Undamped Oscillations

The electrical oscillations whose amplitude remains constant with time are called as **Undamped Oscillations**. The frequency of the undamped oscillations remains constant.



Undamped oscillations are generally produced by the oscillatory circuits that produce no power losses and follow compensation techniques if any power losses occur.

An amplifier with positive feedback produces its output to be in phase with the input and increases the strength of the signal. Positive feedback is also called as **degenerative feedback** or**direct feedback**. This kind of feedback makes a feedback amplifier, an oscillator.

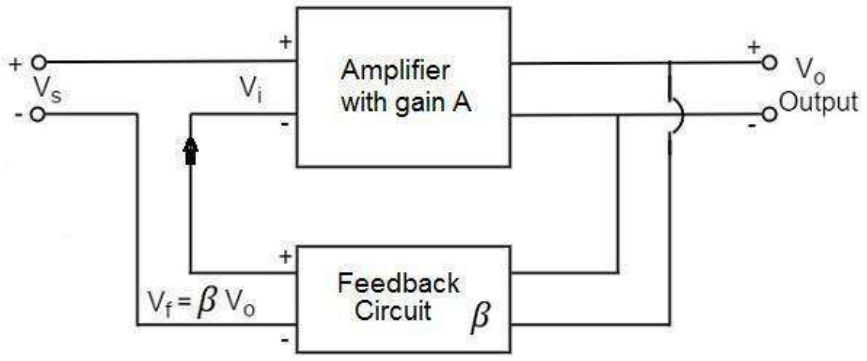
The use of positive feedback results in a feedback amplifier having closed-loop gain greater than the open-loop gain. It results in **instability** and operates as an oscillatory circuit. An oscillatory circuit provides a constantly varying amplified output signal of any desired frequency.

The Barkhausen Criterion

With the knowledge we have till now, we understood that a practical oscillator circuit consists of a tank circuit, a transistor amplifier circuit and a feedback circuit. so, let us now try to brush up the concept of feedback amplifiers, to derive the gain of the feedback amplifiers.

Principle of Feedback Amplifier

A feedback amplifier generally consists of two parts. They are the **amplifier** and the **feedback circuit**. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure below.



From the above figure, the gain of the amplifier is represented as A. The gain of the amplifier is the ratio of output voltage Vo to the input voltage V_i. The feedback network extracts a voltage $V_f = \beta V_o$ from the output V_o of the amplifier.

This voltage is added for positive feedback and subtracted for negative feedback, from the signal voltage V_s.

So, for a positive feedback,

$$V_i = V_s + V_f = V_s + \beta V_o$$

The quantity $\beta = V_f/V_o$ is called as feedback ratio or feedback fraction.

The output V_o must be equal to the input voltage ($V_s + \beta V_o$) multiplied by the gain A of the amplifier.

Hence,

$(Vs+\beta Vo)A=Vo$

Or

$AVs+A\beta Vo=Vo$

Or

$AVs=Vo(1-A\beta)$

Therefore

$$\frac{V_o}{V_s} = \frac{A}{(1-A\beta)}$$

Let A_f be the overall gain (gain with the feedback) of the amplifier. This is defined as the ratio of output voltage V_o to the applied signal voltage V_s, i.e.,

from the above two equations, we can understand that, the equation of gain of the feedback amplifier with positive feedback is given by

$$Af = \frac{A}{1 - A\beta}$$

Where **Aβ** is the **feedback factor** or the **loop gain**.

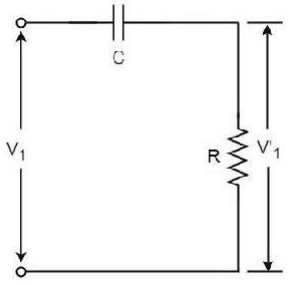
If Aβ = 1, $A_f = \infty$. Thus the gain becomes infinity, i.e., there is output without any input. In another words, the amplifier works as an Oscillator.

The condition Aβ = 1 is called as **Barkhausen Criterion of oscillations**. This is a very important factor to be always kept in mind, in the concept of Oscillators

RC-Phase–shift Oscillators

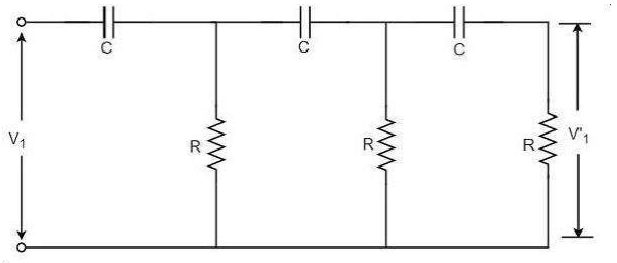
PrincipleofPhase-shiftoscillators

We know that the output voltage of an RC circuit for a sinewave input leads the input voltage. The phase angle by which it leads is determined by the value of RC components used in the circuit. The following circuit diagram shows a single section of an RC network.



The output voltage V_1' across the resistor R leads the input voltage applied input V_1 by some phase angle ϕ^o. If R were reduced to zero, V_1' will lead the V_1 by 90° i.e., ϕ^o=90°.

However, adjusting R to zero would be impracticable, because it would lead to no voltage across R. Therefore, in practice, R is varied to such a value that makes V_1' to lead V_1 by 60°. The following circuit diagram shows the three sections of the RC network.



Each section produces a phase shift of 60°. Consequently, a total phase shift of 180° is produced, i.e., voltage V_2 leads the voltage V_1 by 180°.

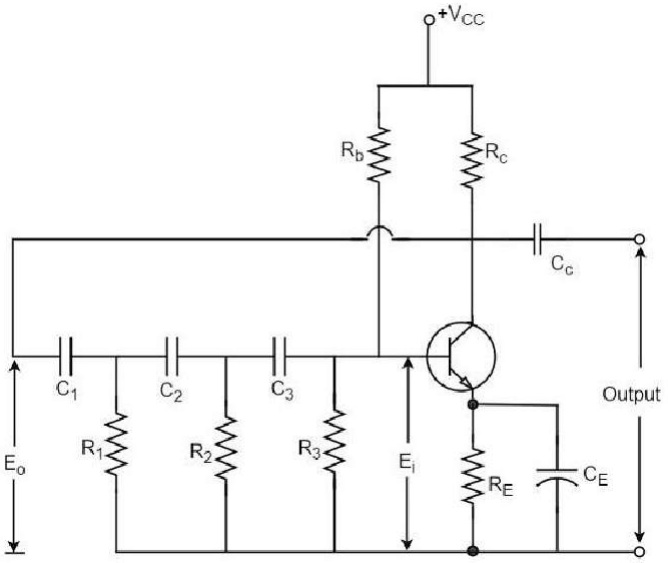
Phase-shift Oscillator Circuit

The oscillator circuit that produces a sine wave using a phase-shift network is called as a Phase-shift oscillator circuit. The constructional details and operation of a phase-shift oscillator circuit are as given below.

Construction

The phase-shift oscillator circuit consists of a single transistor amplifier section and a RC phase-shift network. The phase shift network in this circuit, consists of three RC sections. At the resonant frequency f_o, the phase shift in each RC section is 60° so that the total phase shift produced by RC network is 180°.

The following circuit diagram shows the arrangement of an RC phase-shift oscillator.



The frequency of oscillations is given by

$$f_o = \frac{1}{2\pi RC\sqrt{6}}$$

Where

$$R_1 = R_2 = R_3 = R$$

$$C_1 = C_2 = C_3 = C$$

Operation

The circuit when switched ON oscillates at the resonant frequency f_o. The output E_o of the amplifier is fed back to RC feedback network. This network produces a phase shift of 180^o and a voltage E_i appears at its output. This voltage is applied to the transistor amplifier.

The feedback applied will be

$$m=Ei/Eo$$

The feedback is in correct phase, whereas the transistor amplifier, which is in CE configuration, produces a 180^o phase shift. The phase shift produced by network and the transistor add to form a phase shift around the entire loop which is 360^o.

Advantages

The advantages of RC phase shift oscillator are as follows −

- It does not require transformers or inductors.
- It can be used to produce very low frequencies.
- The circuit provides good frequency stability.

Disadvantages

The disadvantages of RC phase shift oscillator are as follows −

- Starting the oscillations is difficult as the feedback is small.
- The output produced is small.

Another type of popular audio frequency oscillator is the Wien bridge oscillator circuit. This is mostly used because of its important features. This circuit is free from the **circuit fluctuations** and the **ambient temperature**.

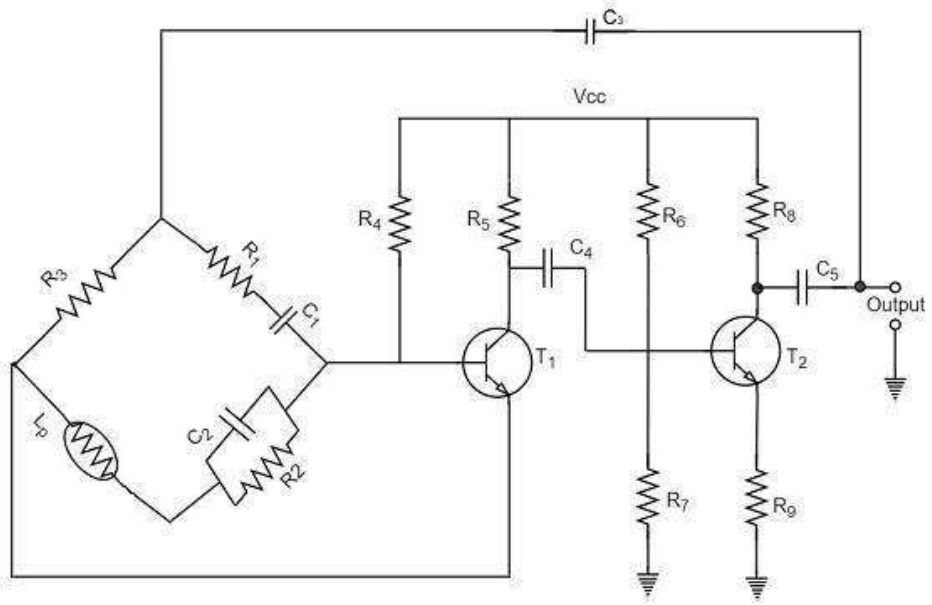
The main advantage of this oscillator is that the frequency can be varied in the range of 10Hz to about 1MHz whereas in RC oscillators, the frequency is not varied.

Wien bridge oscillator

Construction

The circuit construction of Wien bridge oscillator can be explained as below. It is a two-stage amplifier with RC bridge circuit. The bridge circuit has the arms R_1C_1, R_3, R_2C_2 and the tungsten lamp L_p. Resistance R_3 and the lamp L_p are used to stabilize the amplitude of the output.

The following circuit diagram shows the arrangement of a Wien bridge oscillator.



The transistor T_1 serves as an oscillator and an amplifier while the other transistor T_2 serves as an inverter. The inverter operation provides a phase shift of 180°. This circuit provides positive feedback through R_1C_1, C_2R_2 to the transistor T_1 and negative feedback through the voltage divider to the input of transistor T_2.

The frequency of oscillations is determined by the series element R_1C_1 and parallel element R_2C_2 of the bridge.

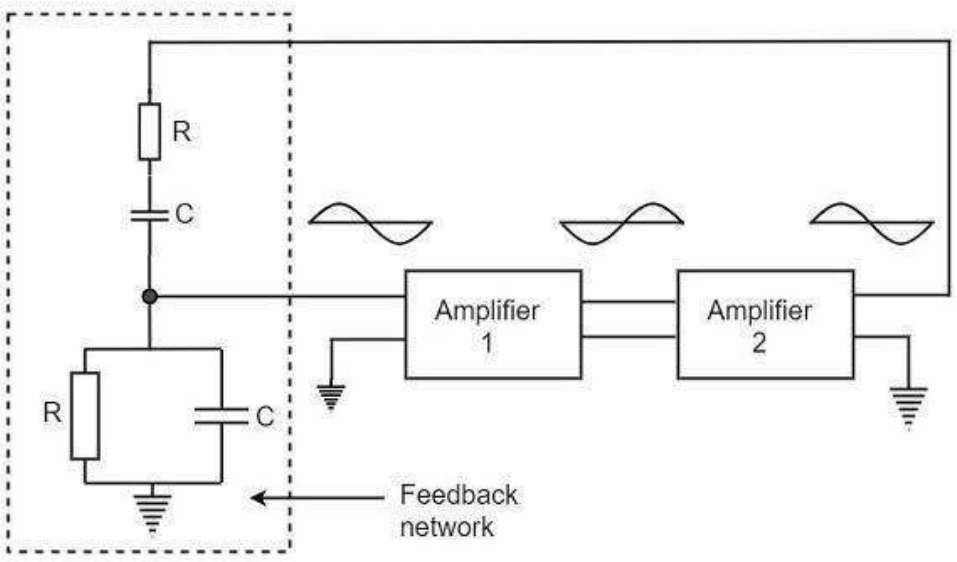
$$f = \frac{1}{2\pi\sqrt{R_1C_1R_2C_2}}$$

If $R_1 = R_2$ and $C_1 = C_2 = C$

Then,

$$f = \frac{1}{2\pi RC}$$

Now, we can simplify the above circuit as follows −



The oscillator consists of two stages of RC coupled amplifier and a feedback network. The voltage across the parallel combination of R and C is fed to the input of amplifier 1. The net phase shift through the two amplifiers is zero.

The usual idea of connecting the output of amplifier 2 to amplifier 1 to provide signal regeneration for oscillator is not applicable here as the amplifier 1 will amplify signals over a wide range of frequencies and hence direct coupling would result in poor frequency stability. By adding Wien bridge feedback network, the oscillator becomes sensitive to a particular frequency and hence frequency stability is achieved.

Operation

When the circuit is switched ON, the bridge circuit produces oscillations of the frequency stated above. The two transistors produce a total phase shift of 360° so that proper positive feedback is ensured. The negative feedback in the circuit ensures constant output. This is achieved by temperature sensitive tungsten lamp L_p. Its resistance increases with current.

If the amplitude of the output increases, more current is produced and more negative feedback is achieved. Due to this, the output would return to the original value. Whereas, if the output tends to decrease, reverse action would take place.

Advantages

The advantages of Wien bridge oscillator are as follows −

- The circuit provides good frequency stability.

- It provides constant output.
- The operation of circuit is quite easy.
- The overall gain is high because of two transistors.
- The frequency of oscillations can be changed easily.
- The amplitude stability of the output voltage can be maintained more accurately, by replacing R_2 with a thermistor.

Disadvantages

The disadvantages of Wien bridge oscillator are as follows −

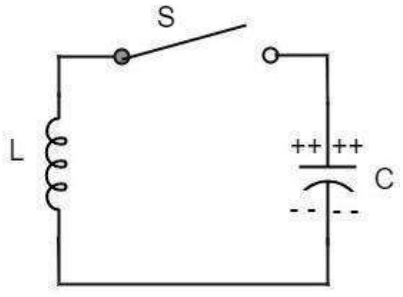
- The circuit cannot generate very high frequencies.
- Two transistors and number of components are required for the circuit construction.

LC Oscillators

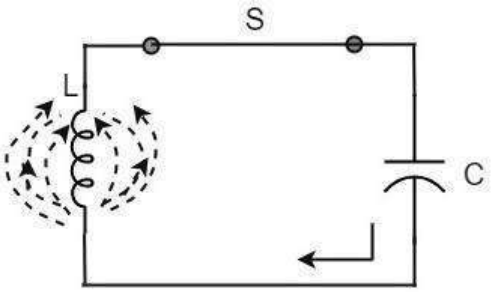
An oscillatory circuit produces electrical oscillations of a desired frequency. They are also known as **tank circuits**.

A simple tank circuit comprises of an inductor L and a capacitor C both of which together determine the oscillatory frequency of the circuit.

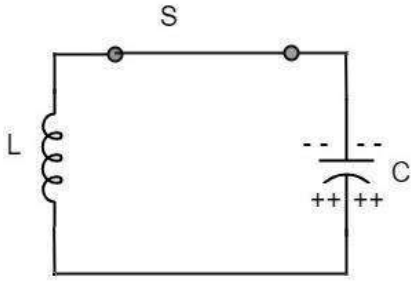
To understand the concept of oscillatory circuit, let us consider the following circuit. The capacitor in this circuit is already charged using a dc source. In this situation, the upper plate of the capacitor has excess of electrons whereas the lower plate has deficit of electrons. The capacitor holds some electrostatic energy and there is a voltage across the capacitor.



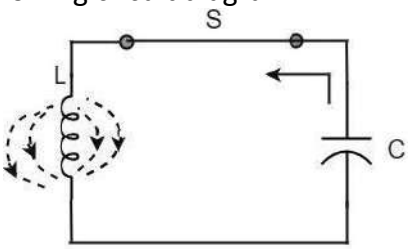
When the switch **S** is closed, the capacitor discharges and the current flows through the inductor. Due to the inductive effect, the current builds up slowly towards a maximum value. Once the capacitor discharges completely, the magnetic field around the coil is maximum.



Now, let us move on to the next stage. Once the capacitor is discharged completely, the magnetic field begins to collapse and produces a counter EMF according to Lenz's law. The capacitor is now charged with positive charge on the upper plate and negative charge on the lower plate.



Once the capacitor is fully charged, it starts to discharge to build up a magnetic field around the coil, as shown in the following circuit diagram.



This continuation of charging and discharging results in alternating motion of electrons or an **oscillatory current**. The interchange of energy between L and C produce continuous **oscillations**.

In an ideal circuit, where there are no losses, the oscillations would continue indefinitely. In a practical tank circuit, there occur losses such as **resistive** and **radiation losses** in the coil and **dielectric losses** in the capacitor. These losses result in damped oscillations.

Frequency of Oscillations

The frequency of the oscillations produced by the tank circuit are determined by the components of the tank circuit, **the L** and **the C**. The actual frequency of oscillations is the **resonant frequency** (or natural frequency) of the tank circuit which is given by

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Capacitance of the capacitor

The frequency of oscillation f_o is inversely proportional to the square root of the capacitance of a capacitor. So, if the value of the capacitor used is large, the charge and discharge time periods will be large. Hence the frequency will be lower.

Mathematically, the frequency,

$$f_o \propto \frac{1}{\sqrt{C}}$$

Self-Inductance of the coil

The frequency of the oscillation f_o is proportional to the square root of the self-inductance of the coil. If the value of the inductance is large, the opposition to change of current flow is greater and hence the time required to complete each cycle will be longer, which means time period will be longer and frequency will be lower.

Mathematically, the frequency,

$$f_o \propto \frac{1}{\sqrt{L}}$$

Combining both the above equations,

$$f_o \propto \frac{1}{\sqrt{LC}}$$

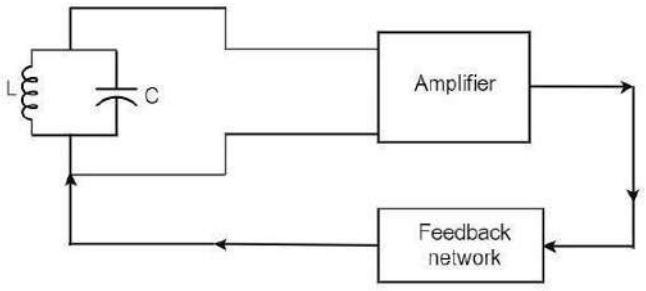
$$f_o = \frac{1}{2\pi\sqrt{LC}}$$

The above equation, though indicates the output frequency, matches the **natural frequency** or **resonance frequency** of the tank circuit.

An Oscillator circuit is a complete set of all the parts of circuit which helps to produce the oscillations. These oscillations should sustain and should be Undamped as just discussed before. Let us try to analyze a practical Oscillator circuit to have a better understanding on how an Oscillator circuit works.

Practical Oscillator Circuit

A Practical Oscillator circuit consists of a tank circuit, a transistor amplifier, and a feedback circuit. The following circuit diagram shows the arrangement of a practical oscillator.



Let us now discuss the parts of this practical oscillator circuit.

Tank Circuit − The tank circuit consists of an inductance L connected in parallel with capacitor **C**. The values of these two components determine the frequency of the oscillator circuit and hence this is called as **Frequency determining circuit**.

- **Transistor Amplifier** − The output of the tank circuit is connected to the amplifier circuit so that the oscillations produced by the tank circuit are amplified here. Hence the output of these oscillations are increased by the amplifier.
- **Feedback Circuit** − The function of feedback circuit is to transfer a part of the output energy to LC circuit in proper phase. This feedback is positive in oscillators while negative in amplifiers.

Frequency Stability of an Oscillator

The frequency stability of an oscillator is a measure of its ability to maintain a constant frequency, over a long time interval. When operated over a longer period of time, the oscillator frequency may have a drift from the previously set value either by increasing or by decreasing.

The change in oscillator frequency may arise due to the following factors −

- Operating point of the active device such as BJT or FET used should lie in the linear region of the amplifier. Its deviation will affect the oscillator frequency.
- The temperature dependency of the performance of circuit components affect the oscillator frequency.
- The changes in d.c. supply voltage applied to the active device, shift the oscillator frequency. This can be avoided if a regulated power supply is used.
- A change in output load may cause a change in the Q-factor of the tank circuit, thereby causing a change in oscillator output frequency.
- The presence of inter element capacitances and stray capacitances affect the oscillator output frequency and thus frequency stability.

Tuned circuit oscillators are the circuits that produce oscillations with the help of tuning circuits. The tuning circuits consists of an inductance L and a capacitor C. These are also known as **LC oscillators, resonant circuit oscillators** or **tank circuit oscillators**.

The tuned circuit oscillators are used to produce an output with frequencies ranging from 1 MHz to 500 MHz Hence these are also known as **R.F. Oscillators**. A BJT or a FET is used as an amplifier with tuned circuit oscillators. With an amplifier and an LC tank circuit, we can feedback a signal with right amplitude and phase to maintain oscillations.

Types of Tuned Circuit Oscillators

Most of the oscillators used in radio transmitters and receivers are of LC oscillators type. Depending upon the way the feedback is used in the circuit, the LC oscillators are divided as the following types.

- **Hartley Oscillator** − It uses inductive feedback.
- **Colpitts Oscillator** − It uses capacitive feedback.

Hartley Oscillator

A very popular **local oscillator** circuit that is mostly used in **radio receivers** is the **Hartley Oscillator** circuit. The constructional details and operation of a Hartley oscillator are as discussed below.

Construction

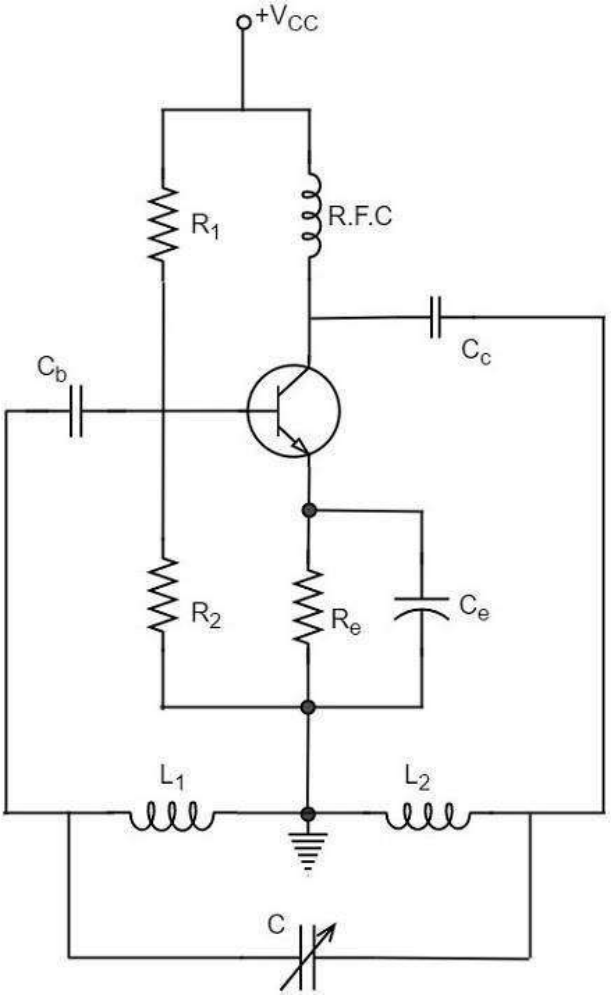
In the circuit diagram of a Hartley oscillator shown below, the resistors R_1, R_2 and R_e provide necessary bias condition for the circuit. The capacitor C_e provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization.

The capacitors C_c and C_b are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source

Tank Circuit

The frequency determining network is a parallel resonant circuit which consists of the inductors L_1 and L_2 along with a variable capacitor C. The junction of L_1 and L_2 are earthed. The coil L_1 has its one end connected to base via C_c and the other to emitter via C_e. So, L_2 is in the output circuit. Both the coils L_1 and L_2 are inductively coupled and together form an **Auto-transformer**.

The following circuit diagram shows the arrangement of a Hartley oscillator. The tank circuit is **shunt fed** in this circuit. It can also be a **series-fed**.



Operation

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across L_1.

The **auto-transformer** made by the inductive coupling of L_1 and L_2 helps in determining the frequency and establishes the feedback. As the CE configured transistor provides 180^o phase shift, another 180^o phase shift is provided by the transformer, which makes 360^o phase shift between the input and outputvoltages.

This makes the feedback positive which is essential for the condition of oscillations. When the **loop gain |βA| of the amplifier is greater than one**, oscillations are sustained in the circuit.

Frequency

The equation for **frequency of Hartley oscillator** is given as

$$f = \frac{1}{2\pi\sqrt{L_T C}}$$

$$L_T = L_1 + L_2 + 2M$$

Here, L_T is the total cumulatively coupled inductance; L_1 and L_2represent inductances of 1st and 2nd coils; and **M** represents mutual inductance.

Mutual inductance is calculated when two windings are considered.

Advantages

The advantages of Hartley oscillator are

- Instead of using a large transformer, a single coil can be used as an auto-transformer.
- Frequency can be varied by employing either a variable capacitor or a variable inductor.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequencyrange.

Disadvantages

The disadvantages of Hartley oscillator are

- It cannot be a low frequency oscillator.
- Harmonic distortions are present.

Applications

The applications of Hartley oscillator are

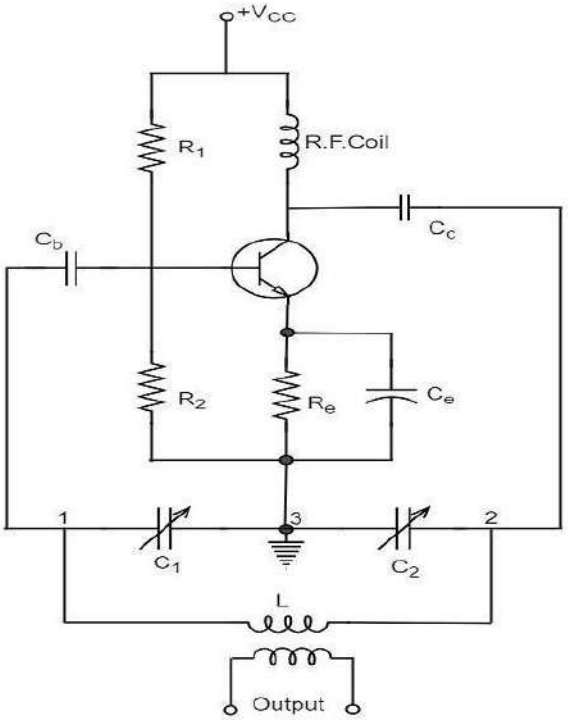
- It is used to produce a sine wave of desired frequency.
- Mostly used as a local oscillator in radio receivers.
- It is also used as R.F. Oscillator.

Colpitts oscillator

A Colpitts oscillator looks just like the Hartley oscillator but the inductors and capacitors are replaced with each other in the tank circuit. The constructional details and operation of a colpitts oscillator are as discussed below.

Construction

Let us first take a look at the circuit diagram of a Colpitts oscillator.



The resistors R_1, R_2 and R_e provide necessary bias condition for the circuit. The capacitor C_e provides a.c. ground thereby providing any signal degeneration. This also provides temperature stabilization.

The capacitors C_c and C_b are employed to block d.c. and to provide an a.c. path. The radio frequency choke (R.F.C) offers very high impedance to high frequency currents which means it shorts for d.c. and opens for a.c. Hence it provides d.c. load for collector and keeps a.c. currents out of d.c. supply source.

Tank Circuit

The frequency determining network is a parallel resonant circuit which consists of variable capacitors C_1 and C_2 along with an inductor L. The junction of C_1 and C_2 are earthed. The capacitor C_1 has its one end connected to base via C_c and the other to emitter via C_e. the voltage developed across C_1 provides the regenerative feedback required for the sustained oscillations.

Operation

When the collector supply is given, a transient current is produced in the oscillatory or tank circuit. The oscillatory current in the tank circuit produces a.c. voltage across C_1 which are

applied to the base emitter junction and appear in the amplified form in the collector circuit and supply losses to the tank circuit.

If terminal 1 is at positive potential with respect to terminal 3 at any instant, then terminal 2 will be at negative potential with respect to 3 at that instant because terminal 3 is grounded. Therefore, points 1 and 2 are out of phase by 180°.

As the CE configured transistor provides 180° phase shift, it makes 360° phase shift between the input and output voltages. Hence, feedback is properly phased to produce continuous Undamped oscillations. When the **loop gain |βA| of the amplifier is greater than one, oscillations are sustained** in the circuit.

Frequency

The equation for **frequency of Colpitts oscillator** is given as

$$f = \frac{1}{2\pi\sqrt{LC_T}}$$

C_T is the total capacitance of C_1 and C_2 connected in series.

$$\frac{1}{C_T} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$C_T = \frac{C_1 \times C_2}{C_1 + C_2}$$

Advantages

The advantages of Colpitts oscillator are as follows −

- Colpitts oscillator can generate sinusoidal signals of very high frequencies.
- It can withstand high and low temperatures.
- The frequency stability is high.
- Frequency can be varied by using both the variable capacitors.
- Less number of components are sufficient.
- The amplitude of the output remains constant over a fixed frequency range.

The Colpitts oscillator is designed to eliminate the disadvantages of Hartley oscillator and is known to have no specific disadvantages. Hence there are many applications of a colpitts oscillator.

Applications

The applications of Colpitts oscillator are as follows −

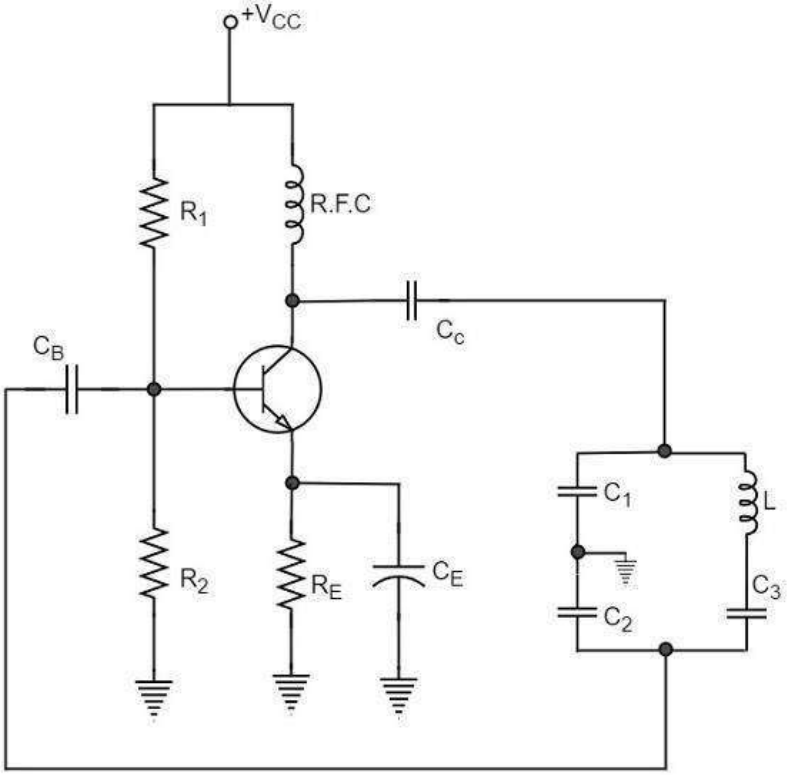
- Colpitts oscillator can be used as High frequency sinewave generator.
- This can be used as a temperature sensor with some associated circuitry.
- Mostly used as a local oscillator in radio receivers.
- It is also used as R.F. Oscillator.
- It is also used in Mobile applications.
- It has got many other commercial applications.

Clapp Oscillator

Another oscillator which is an advanced version of Colpitts oscillator is the **Clapp Oscillator**. This circuit is designed by making a few changes to the Colpitts oscillator.

The circuit differs from the Colpitts oscillator only in one respect; it contains one additional capacitor (C_3) connected in series with the inductor. The addition of capacitor (C_3) improves the frequency stability and eliminates the effect of transistor parameters and stray capacitances.

The following circuit diagram shows the arrangement of a**transistor Clapp oscillator**.



The operation of Clapp oscillator circuit is in the same way as that of Colpitts oscillator. The frequency of oscillator is given by the relation,

$$f_o = \frac{1}{2\pi\sqrt{L.C}}$$

Where

$$C = \frac{1}{\frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}}$$

Usually, the value of $\mathbf{C_3}$ is much smaller than $\mathbf{C_1}$ and $\mathbf{C_2}$. As a result of this, **C** is approximately equal to $\mathbf{C_3}$. Therefore, the frequency of oscillation,

$$f_o = \frac{1}{2\pi\sqrt{L.C_3}}$$

It is understood that the Clapp oscillator is similar to the Colpitts oscillator, however they differ in the way the inductances and capacitances are arranged. The frequency stability though is good, can be variable in a Clapp oscillator.

A Clapp oscillator is sometimes preferred over a Colpitts oscillator for constructing a variable frequency oscillator. The Clapp oscillators are used in receiver tuning circuits as a frequency oscillator.

One of the important features of an oscillator is that the feedback energy applied should be in correct phase to the tank circuit. The oscillator circuits discussed so far has employed inductor (L) and capacitor (C) combination, in the tank circuit or frequency determining circuit.

We have observed that the LC combination in oscillators provide 180° phase shift and transistor in CE configuration provide 180° phase shift to make a total of 360° phase shift so that it would make a zero difference in phase.

Drawbacks of LC circuits

Though they have few applications, the **LC** circuits have few **drawbacks** such as

- Frequency instability
- Waveform is poor
- Cannot be used for low frequencies
- Inductors are bulky and expensive

Whenever an oscillator is under continuous operation, its **frequency stability** gets affected. There occur changes in its frequency. The main factors that affect the frequency of an oscillator are

- Power supply variations
- Changes in temperature
- Changes in load or output resistance

In RC and LC oscillators the values of resistance, capacitance and inductance vary with temperature and hence the frequency gets affected. In order to avoid this problem, the piezo electric crystals are being used in oscillators.

Crystal Oscillators

The use of piezo electric crystals in parallel resonant circuits provide high frequency stability in oscillators. Such oscillators are called as **Crystal Oscillators**.

Crystal Oscillators

The principle of crystal oscillators depends upon the **Piezo electric effect**. The natural shape of a crystal is hexagonal. When a crystal wafer is cur perpendicular to X-axis, it is called as X-cut and when it is cut along Y-axis, it is called as Y-cut.

The crystal used in crystal oscillator exhibits a property called as Piezo electric property. So, let us have an idea on piezo electric effect.

Piezo Electric Effect

The crystal exhibits the property that when a mechanical stress is applied across one of the faces of the crystal, a potential difference is developed across the opposite faces of the crystal. Conversely, when a potential difference is applied across one of the faces, a mechanical stress is produced along the other faces. This is known as **Piezo electric effect**.

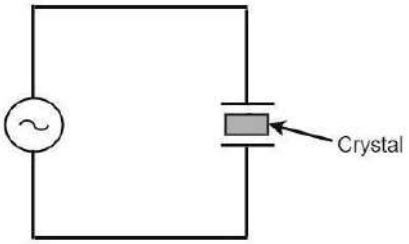
Certain crystalline materials like Rochelle salt, quartz and tourmaline exhibit piezo electric effect and such materials are called as **Piezo electric crystals**. Quartz is the most commonly used piezo electric crystal because it is inexpensive and readily available in nature.

When a piezo electric crystal is subjected to a proper alternating potential, it vibrates mechanically. The amplitude of mechanical vibrations becomes maximum when the frequency of alternating voltage is equal to the natural frequency of the crystal.

Working of a Quartz Crystal

In order to make a crystal work in an electronic circuit, the crystal is placed between two metal plates in the form of a capacitor. **Quartz** is the mostly used type of crystal because of its availability and strong nature while being inexpensive. The ac voltage is applied in parallel to the crystal.

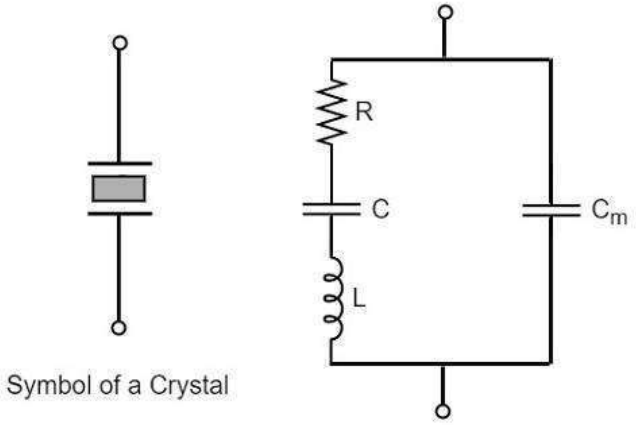
The circuit arrangement of a Quartz Crystal will be as shown below −



If an AC voltage is applied, the crystal starts vibrating at the frequency of the applied voltage. However, if the frequency of the applied voltage is made equal to the natural frequency of the crystal, **resonance** takes place and crystal vibrations reach a maximum value. This natural frequency is almost constant.

Equivalent circuit of a Crystal

If we try to represent the crystal with an equivalent electric circuit, we have to consider two cases, i.e., when it vibrates and when it doesn't. The figures below represent the symbol and electrical equivalent circuit of a crystal respectively.



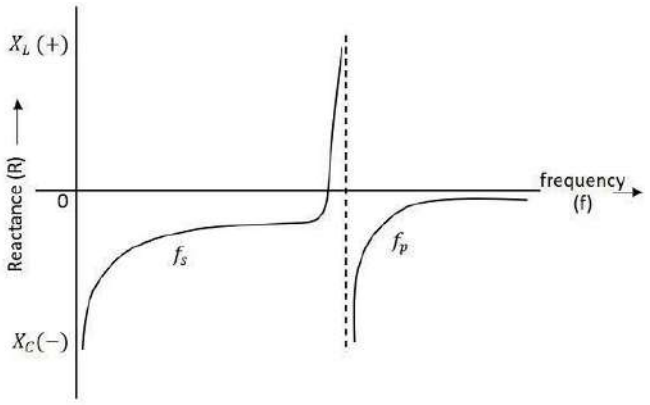
Symbol of a Crystal

Equivalent circuit of a crystal

The above equivalent circuit consists of a series R-L-C circuit in parallel with a capacitance C_m. When the crystal mounted across the AC source is not vibrating, it is equivalent to the capacitance C_m. When the crystal vibrates, it acts like a tuned R-L-C circuit.

Frequency response

The frequency response of a crystal is as shown below. The graph shows the reactance (X_L or X_C) versus frequency (f). It is evident that the crystal has two closely spaced resonant frequencies.



The first one is the series resonant frequency (f_s), which occurs when reactance of the inductance (L) is equal to the reactance of the capacitance C. In that case, the impedance of the equivalent circuit is equal to the resistance R and the frequency of oscillation is given by the relation,

$$f = \frac{1}{2\pi\sqrt{L.C}}$$

The second one is the parallel resonant frequency (f_p), which occurs when the reactance of R-L-C branch is equal to the reactance of capacitor C_m. At this frequency, the crystal offers a very high impedance to the external circuit and the frequency of oscillation is given by the relation.

$$f_p = \frac{1}{2\pi\sqrt{L.C_T}}$$

Where

$$C_T = \frac{CC_m}{(C + C_m)}$$

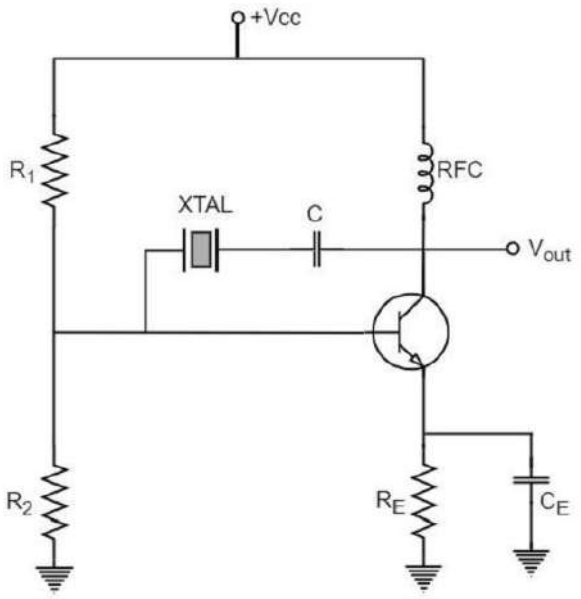
The value of C_m is usually very large as compared to C. Therefore, the value of C_T is approximately equal to C and hence the series resonant frequency is approximately equal to the parallel resonant frequency (i.e., $f_s = f_p$).

Crystal Oscillator Circuit

pierce crystal oscillator

A crystal oscillator circuit can be constructed in a number of ways like a Crystal controlled tuned collector oscillator, a Colpitts crystal oscillator, a Clap crystal oscillator etc. But the **transistor pierce crystal oscillator** is the most commonly used one. This is the circuit which is normally referred as a crystal oscillator circuit.

The following circuit diagram shows the arrangement of a transistor pierce crystal oscillator.



In this circuit, the crystal is connected as a series element in the feedback path from collector to the base. The resistors R_1, R_2 and R_E provide a voltage-divider stabilized d.c. bias circuit. The capacitor C_E provides a.c. bypass of the emitter resistor and RFC (radio frequency choke) coil provides for d.c. bias while decoupling any a.c. signal on the power lines from affecting the output signal. The coupling capacitor C has negligible impedance at the circuit operating frequency. But it blocks any d.c. between collector and base.

The circuit frequency of oscillation is set by the series resonant frequency of the crystal and its value is given by the relation,

$$f = \frac{1}{2\pi\sqrt{L.C}}$$

It may be noted that the changes in supply voltage, transistor device parameters etc. have no effect on the circuit operating frequency, which is held stabilized by the crystal.

Advantages

The advantages of crystal oscillator are as follows −

- They have a high order of frequency stability.
- The quality factor (Q) of the crystal is very high.

Disadvantages

The disadvantages of crystal oscillator are as follows −

- They are fragile and can be used in low power circuits.
- The frequency of oscillations cannot be changedappreciably.

FrequencyStabilityof an Oscillator

An Oscillator is expected to maintain its frequency for a longer duration without any variations, so as to have a smoother clear sinewave output for the circuit operation. Hence the term frequency stability really matters a lot, when it comes to oscillators, whether sinusoidal or non-sinusoidal.

The frequency stability of an oscillator is defined as the ability of the oscillator to maintain the required frequency constant over a long time interval as possible. Let us try to discuss the factors that affect this frequency stability.

Change in operating point

We have already come across the transistor parameters and learnt how important an operating point is. The stability of this operating point for the transistor being used in the circuit for amplification (BJT or FET), is of higher consideration.

The operating of the active device used is adjusted to be in the linear portion of its characteristics. This point is shifted due to temperature variations and hence the stability is affected.

Variation in temperature

The tank circuit in the oscillator circuit, contains various frequency determining components such as resistors, capacitors and inductors. All of their parameters are temperature dependent. Due to the change in temperature, their values get affected. This brings the change in frequency of the oscillator circuit.

Due to power supply

The variations in the supplied power will also affect the frequency. The power supply variations lead to the variations in V_{cc}. This will affect the frequency of the oscillations produced.

In order to avoid this, the regulated power supply system is implemented. This is in short called as RPS.

Change in output load

The variations in output resistance or output load also affects the frequency of the oscillator. When a load is connected, the effective resistance of the tank circuit is changed. As a result, the Q-factor of LC tuned circuit is changed. This results a change in output frequency of oscillator.

Changes in inter-element capacitances

Inter-element capacitances are the capacitances that develop in PN junction materials such as diodes and transistors. These are developed due to the charge present in them during their operation.

The inter element capacitors undergo change due to various reasons as temperature, voltage etc. This problem can be solved by connecting swamping capacitor across offending inter-element capacitor.

Value of Q

The value of Q (Quality factor) must be high in oscillators. The value of Q in tuned oscillators determine the selectivity. As this Q is directly proportional to the frequency stability of a tuned circuit, the value of Q should be maintained high.

Frequency stability can be mathematically represented as,

$$Sw=d\theta/dw$$

Where $d\theta$ is the phase shift introduced for a small frequency change in nominal frequency f_r. The circuit giving the larger value of $(d\theta/dw)$ has more stable oscillatory frequency.

UNIT-5

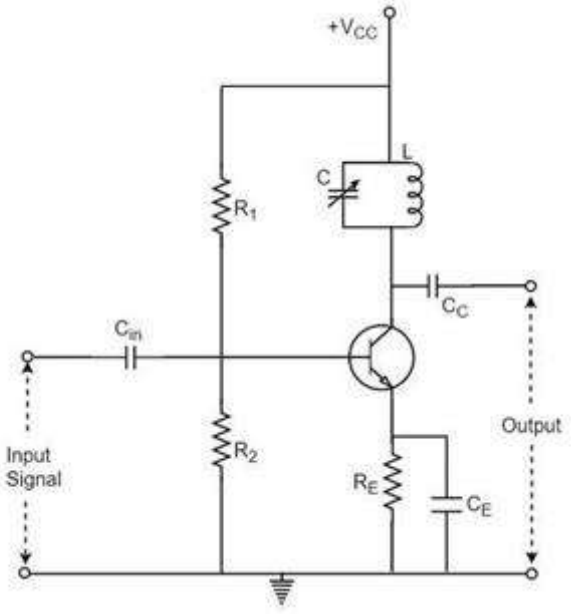
Single Tuned Amplifier

An amplifier circuit with a single tuner section being at the collector of the amplifier circuit is called as Single tuner amplifier circuit.

Construction

A simple transistor amplifier circuit consisting of a parallel tuned circuit in its collector load, makes a single tuned amplifier circuit. The values of capacitance and inductance of the tuned circuit are selected such that its resonant frequency is equal to the frequency to be amplified.

The following circuit diagram shows a single tuned amplifier circuit.



The output can be obtained from the coupling capacitor C_C as shown above or from a secondary winding placed at L.

Operation

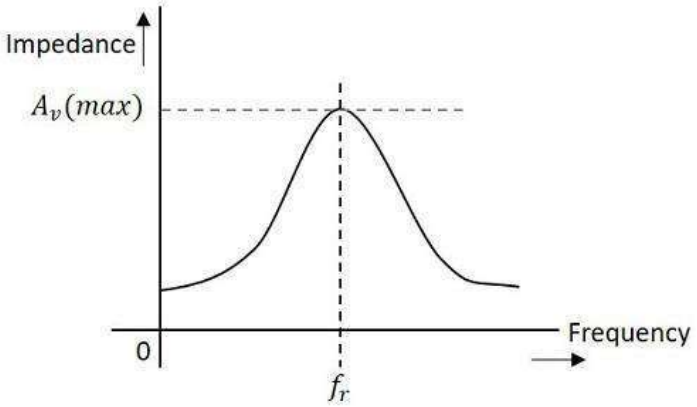
The high frequency signal that has to be amplified is applied at the input of the amplifier. The resonant frequency of the parallel tuned circuit is made equal to the frequency of the signal applied by altering the capacitance value of the capacitor C, in the tuned circuit.At this stage, the tuned circuit offers high impedance to the signal frequency, which helps to offer high output across the tuned circuit. As high impedance is offered only for the tuned frequency, all the other frequencies which get lower impedance are rejected by the tuned circuit. Hence the tuned amplifier selects and amplifies the desired frequency signal.

Frequency Response

The parallel resonance occurs at resonant frequency f_r when the circuit has a high Q. the resonant frequency f_r is given by

$$fr=1/\sqrt{2\pi LC}$$

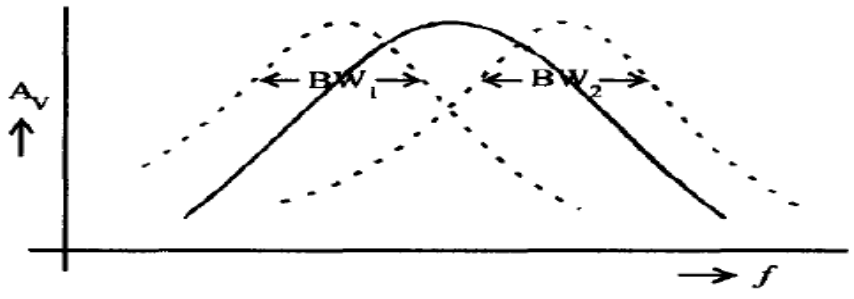
The following graph shows the frequency response of a single tuned amplifier circuit.



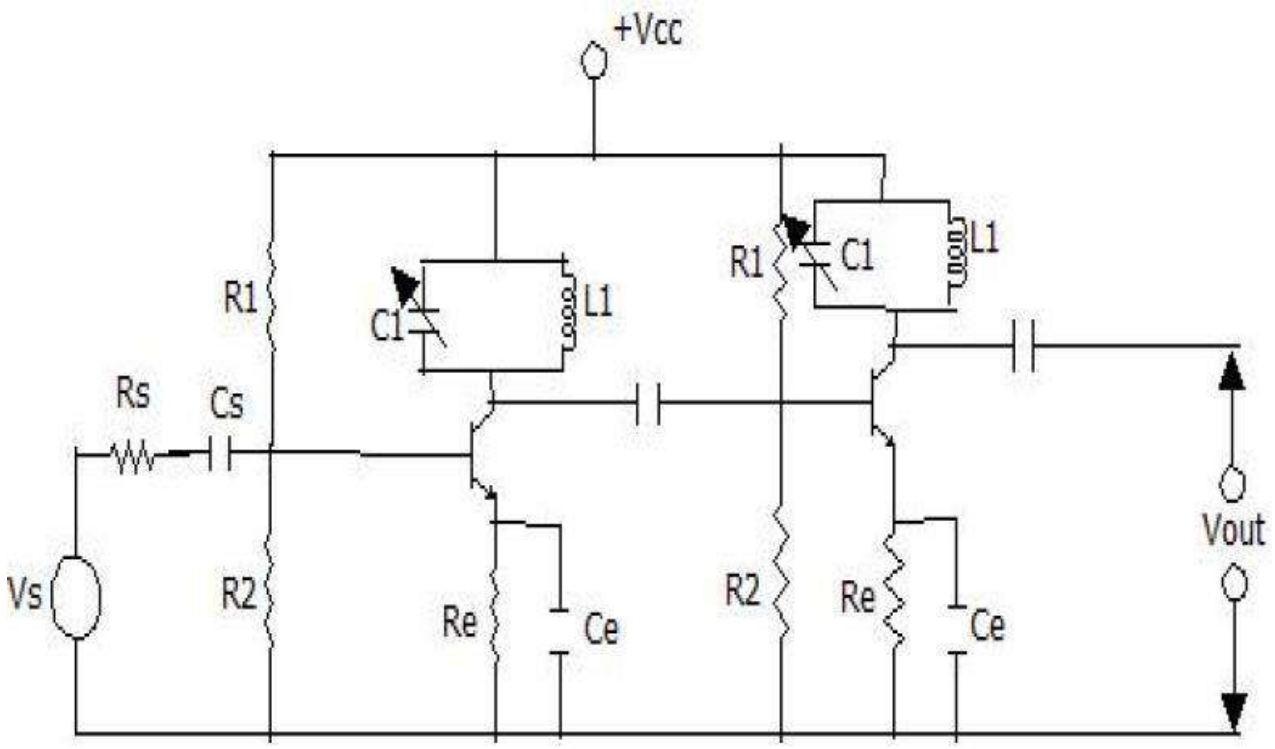
At resonant frequency f_r the impedance of parallel tuned circuit is very high and is purely resistive. The voltage across R_L is therefore maximum, when the circuit is tuned to resonant frequency. Hence the voltage gain is maximum at resonant frequency and drops off above and below it. The higher the Q, the narrower will the curve be.

Stagger Tuning

Tuned amplifiers have large gain, since at resonance, Z is maximum. So Av is maximum. To get this large Av over a wide range of frequencies, stagger tuned amplifiers are employed. This is done by taking two single tuned circuits of a certain Bandwidth, and displacing or staggering their resonance peaks by an amount equal to their Bandwidth. The resultant staggered pair will have a Bandwidth, $\sqrt{2}$ times as great as that of each of individual pairs.



The circuit of stagger tuned amplifier is as shown below:



Stagger Tuned Amplifiers are used to improve the overall frequency response of tuned Amplifiers. Stagger tuned Amplifiers are usually designed so that the overall response exhibits maximal flatness around the centre frequency.

It needs a number of tuned circuit operating in union. The overall frequency response of a Stagger tuned amplifier is obtained by adding the individual response together. Since the resonant Frequencies of different tuned circuits are displaced or staggered, they are referred as Stagger Tuned Amplifier.

The main advantage of stagger tuned amplifier is increased bandwidth. Its Drawback is Reduced Selectivity and critical tuning of many tank circuits. They are used in RF amplifier stage in Radio Receivers.

The stagger tuning in this circuit is achieved by resonating the tuned circuits L1 C1, L2 C2 to slightly different Frequencies

MULTIVIBRATORS

Multi means many; vibrator means oscillator. A circuit which can oscillate at a number of frequencies is called a multivibrator. Basically there are three types of multivibrators:

1. Bistable multivibrator
2. Monostable multivibrator
3. Astable multivibrator

Each of these multivibrators has two states. As the names indicate, a bistable multivibrator has got two stable states, a monostable multivibrator has got only one stable state (the other state being quasi stable) and the astable multivibrator has got no stable state (both the

states being quasi stable). The stable state of a multivibrator is the state in which the device can stay permanently. Only when a proper external triggering signal is applied, it will change its state. Quasi stable state means temporarily stable state. The device cannot stay permanently in this state. After a predetermined time, the device will automatically come out of the quasi stable state.

Multivibrators find applications in a variety of systems where square waves or timed intervals are required. For example, before the advent of low-cost integrated circuits, chains of multivibrators found use as frequency dividers. A free-running multivibrator with a frequency of one-half to one-tenth of the reference frequency would accurately lock to the reference frequency. This technique was used in early electronic organs, to keep notes of different octaves accurately in tune. Other applications included early television systems, where the various line and frame frequencies were kept synchronized by pulses included in the video signal.

BISTABLE MULTIVIBRATOR

A bistable multivibrator is a multivibrator which can exist indefinitely in either of its two stable states and which can be induced to make an abrupt transition from one state to the other by means of external excitation. In a bistable multivibrator both the coupling elements are resistors (dc coupling). The bistable multivibrator is also called a multi, Eccles-Jordan circuit (after its inventors), trigger circuit, scale-of-two toggle circuit, flip-flop, and binary. There are two types of bistable multivibrators:

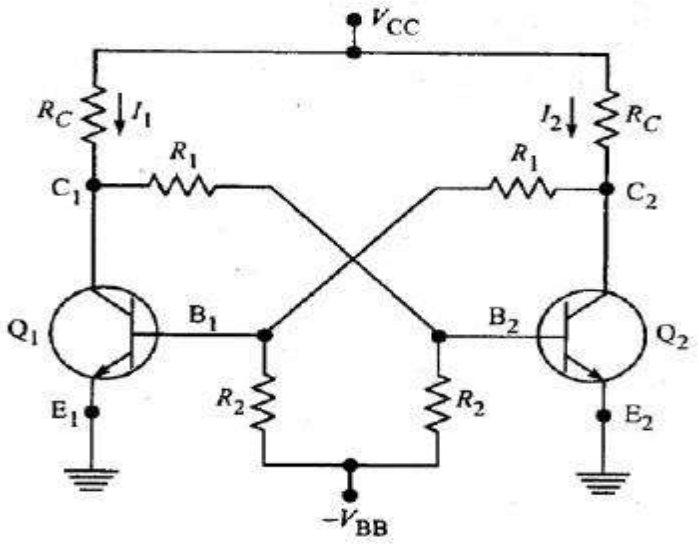
1. Collector coupled bistable multivibrator
2. Emitter coupled bistable multivibrator

There are two types of collector-coupled bistable multivibrators:

1. Fixed-bias bistable multivibrator
2. Self-bias bistable multivibrator

A FIXED-BIAS BISTABLE MULTIVIBRATOR

The Figure below shows the circuit diagram of a fixed-bias bistable multivibrator using transistors (inverters). Note, that the output of each amplifier is direct coupled to the input of the other amplifier.



In one of the stable states, transistor Q[is ON (i.e. in saturation) and Q2 is OFF (i.e. in cut-off), and in the other stable state Qj is OFF and Q2 is ON. Even though the circuit is symmetrical, it is not possible for the circuit to remain in a stable state with both the transistors conducting (i.e. both operating in the active region) simultaneously and carrying equal currents. The reason is that if we assume that both the transistors are biased equally and are carrying equal currents /[and 72 and suppose there is a minute fluctuation in the current *1*\~—let us say it increases by a small amount—then the voltage at the collector of Qi decreases. This will result in a decrease in voltage at the base of Q2. So Q2 conducts less and /2 decreases and hence the potential at the collector of Q2 increases. This results in an increase in the base potential of *Qi.* So, Qi conducts still more and /[is further increased and the potential at the collector of Qt is further reduced, and so on. So, the current *I*\ keeps on increasing and the current /2 keeps on decreasing till Q(goes into saturation and Q2 goes into cut-off. This action takes place because of the regenerative feedback incorporated into the circuit and will occur only if the loop gain is greater than one. *A stable state of a binary is one in which the voltages and currents satisfy the Kirchhoff's laws and are consistent with the device characteristics and in which, in addition, the condition of the loop gain being less than unity is satisfied.*

The condition with respect to loop gain will certainly be satisfied, if either of the two devices is below cut-off or if either device is in saturation. But normally the circuit is designed such that in a stable state one transistor is in saturation and the other one is ir cut-off, because if one transistor is biased to be in cut-off and the other one to be in active region, as the temperature changes or the devices age and the device parameters vary, the quiescent point changes and the quiescent output voltage may also change appreciably Sometimes the drift may

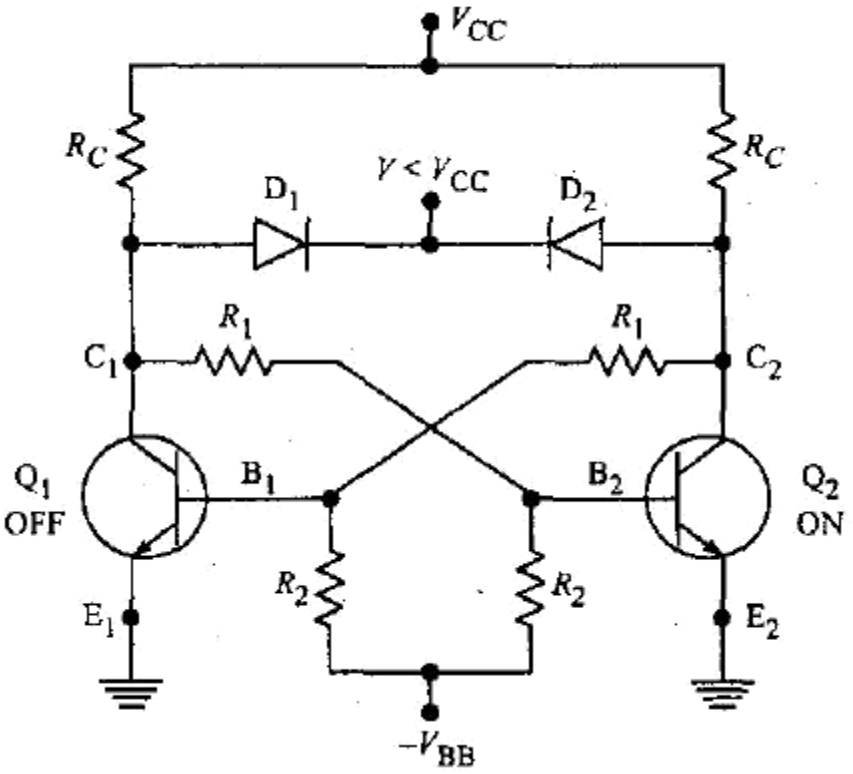
be so much that the device operating in the active region may gc into cut-off, and with both the devices in cut-off the circuit will be useless.

Selection of components in the fixed-bias bistable multivibrator

In the fixed-bias binary shown in Figure 4.1., nearly the full supply voltage Vcc will appear across the transistor that is OFF. Since this supply voltage *Vcc* is to be reasonably smaller than the collector breakdown voltage SVce. *Vcc* restricted to a maximum of a few tens of volts. Under saturation conditions the collector current *Ic* is maximum. Hence *RC* must be chosen so that this value of C (= VCC/^G) does not exceed the maximum permissible limit. The values of *R1, R2* and VBB must be selected such that in one stat>le state the base current is large enough to drive the transistor into saturation whereas in the second stable state the emitter junction must be below cut-off. The signal at a collector called the output swing Vw is the change in collector voltage resulting from a transistor going from one state to the other, i.e. Vw = VCi - IC2- If the loading caused by *RI* can be neglected, then the collector voltage of the OFF transistor is *Vcc.* Since the collector saturation voltage is few tenths of a volt, then the swing Vw = *Vcc,* independently of *RQ*- The component values, the supply voltages and the values of /CBO, *h^,* VBE(sat), and VCE(sat) are sufficient for the analysis of transistor binary circuits.

Loading

The bistable multivibrator may be used to drive other circuits and hence at one or both the collectors there are shunting loads, which are not shown in Figure 4.1. These loads reduce the magnitude of the collector voltage VC1 of the OFF transistor. This will result in reduction of the output voltage swing. A reduced VC[will decrease VB2 and it is possible that Q2 may not be driven into saturation- Hence the flip-flop circuit components must be chosen such that under the heaviest load, which the binary drives, one- transistor remains in saturation while the other is in cut-off. Since the resistor *RI* also loads the OFF transistor, to reduce loading, the value of *R]* should be as large as possible compared to the value of *Rc.* But to ensure a loop gain in excess of unity during the transition between the states, *R^* should be selected such that For some applications, the loading varies with the operation being performed. In such cases, the extent to which a transistor is driven into saturation is variable. A constant output swing V\v = V, arid a constant base saturation current *IB2* can be obtained by clamping the collectors to an auxiliary voltage V < Vcc through the diodes *DI* and D2 as indicated in Figure 4.2. As Qi cuts OFF, its collector voltage rises and when it reaches *V,* the "collector catching diode" D| conducts and clamps the output to *V*.



Standard specifications

In the cut-off region, i.e. for the OFF state

V_{BE} (cut-off) : $\leq$ 0 V for silicon transistor
$\leq$ – 0.1 V for germanium transistor

In the saturation region, i.e. for the ON state

V_{BE} (sat) : 0.7 V for silicon transistor
0.3 V for germanium transistor
V_{CE} (sat) : 0.3 V for silicon transistor
0.1 V for germanium transistor

The above values hold good for n-p-n transistors. For p-n-p transistors the above values with opposite sign are to be taken.

Test for saturation

To test whether a transistor is really in saturation or not evaluate the collector current i_C and the base current i_B independently.

If $i_B > i_B$ (min), where i_B (min) = i_C/h_{FE} (min) the transistor is really in saturation.
If $i_B \leq i_B$ (min), the transistor is not in saturation.

Test for cut-off

To test whether a transistor is really cut-off or not, find its base-to-emitter voltage. If V_{BE} is negative for an n-p-n transistor or positive for a p-n-p transistor, the transistor is really cut-off.

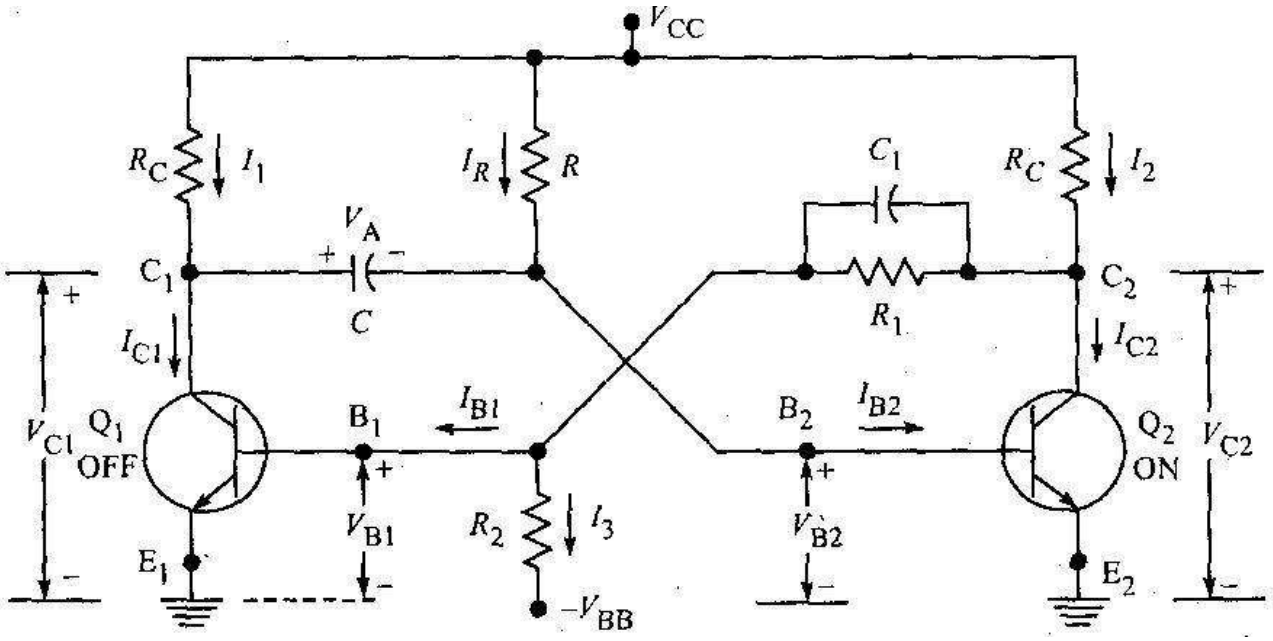
MONOSTABLE MULTIVIBRATOR

Monostable Multivibrators have only **one** stable state (hence their name: "Mono"), and produce a single output pulse when it is triggered externally. Monostable multivibrators only return back to their first original and stable state after a period of time determined by the time constant of the RC coupled circuit.

Monostable multivibrators or "One-Shot Multivibrators" as they are also called, are used to generate a single output pulse of a specified width, either "HIGH" or "LOW" when a suitable external trigger signal or pulse T is applied. This trigger signal initiates a timing cycle which causes the output of the monostable to change its state at the start of the timing cycle and will remain in this second state, which is determined by the time constant of the timing capacitor, CT and the resistor, RT until it resets or returns itself back to its original (stable) state. It will then remain in this original stable state indefinitely until another input pulse or trigger signal is received. Then, **Monostable Multivibrators** have only **ONE** stable state and go through a full cycle in response to a single triggering input pulse.

THE COLLECTOR COUPLED MONOSTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-to-base coupled (simply called collectorcoupled) monostable multivibrator using n-p-n transistors. The collector of Q2 is coupled to the base of Qi by a resistor *R}* (dc coupling) and the collector of Qt is coupled to the base of Q2 by a capacitor *C* (ac coupling). Ci is the commutating capacitor introduced to increase the speed of operation. The base of Qi is connected to -VBB through a resistor *R2,* to ensure that Q! is cut off under quiescent conditions. The base of Q2 is connected to VCc through *R* to ensure that Q2 is ON under quiescent conditions. In fact, *R* may be returned to even a small positive voltage but connecting it to *Vcc* is advantageous. The circuit parameters are selected such that under quiescent conditions, the monostable multivibrator finds itself in its permanent stable state with Q2ON (i.e. in saturation) and Q! OFF (i.e. in cut-off)- The multivibrator may be induced to make a transition out of its stable state by the application of a negative trigger at the base of Q2 or at the collector of Q|. Since the triggering signal is applied to only one device and not to both the devices simultaneously, unsymmetrical triggering is employed. When a negative signal is applied at the base of Q2 at $t \sim 0$, due to regenerative action Q2 goes to OFF state and Qi goes to ON state. When Q, is ON, a current /i flows through its *Rc* and hence its collector voltage drops suddenly by *I\RC* This drop will be instantaneously



transmitted through the coupling capacitor C to the base of Q2. So at t = 0+ , the base voltage of Q2 is

$$V_{BE}(\text{sat}) - I_1 R_C$$

The circuit cannot remain in this state for a long time (it stays in this state only for a finite time *T)* because when Qt conducts, the coupling capacitor *C* charges from Vcc through the conducting transistor Qi and hence the potential at the base of Q2 rises exponentially with a time constant

$(R + R_o)C \approx RC,$ where *R0* is the conducting transistor output impedance including the resistance *Rc.* When it passes the cut-in voltage Vy of Q2 (at a time *t = T),* a regenerative action takes place turning Q| OFF and eventually returning the multivibrator to its initial stable state. The transition from the stable state to the quasi-stable state takes place at *t* = 0, and the reverse transition from the quasi-stable state to the stable state takes place at *t = T.* The time *T* for which the circuit is in its quasi-stable state is also referred to as the delay time, and also as the gate width, pulse width, or pulse duration. The delay time may be varied by varying the time constant *t(= RC).*

Expression for the gate width T of a monostable multivibrator neglecting the reverse saturation current /CBO

The below Figure (a) shows the waveform at the base of transistor Q2 of the monostable multivibrator

For *t* < 0, Q2 is ON and so vB2 = VBE(sat). At *t* = 0, a negative signal applied brings Q2 to OFF state and Q[into saturation. A current I flows through *Rc* of Qt and hence vci drops abruptly by I c volts and so vB2 also drops by *I\RC* instantaneously. So at *t* - 0, vB2 = VBE(sat) - *I}RC.* For *t* > 0, the capacitor charges with a time constant *RC,* and hence the base voltage of Q2 rises exponentially towards VCc with the same time constant. At *t* = *T,* when this base voltage rises to the cut-in voltage level Vy of the transistor, Q2 goes to ON state, and Qj to OFF state and the pulse ends. In the interval 0 < *t* < 7", the base voltage of Q2, i.e. vB2 is given by

$$v_{B2} = V_{CC} - (V_{CC} - \{V_{BE}(\text{sat}) - I_1 R_C\})e^{-t/\tau}$$

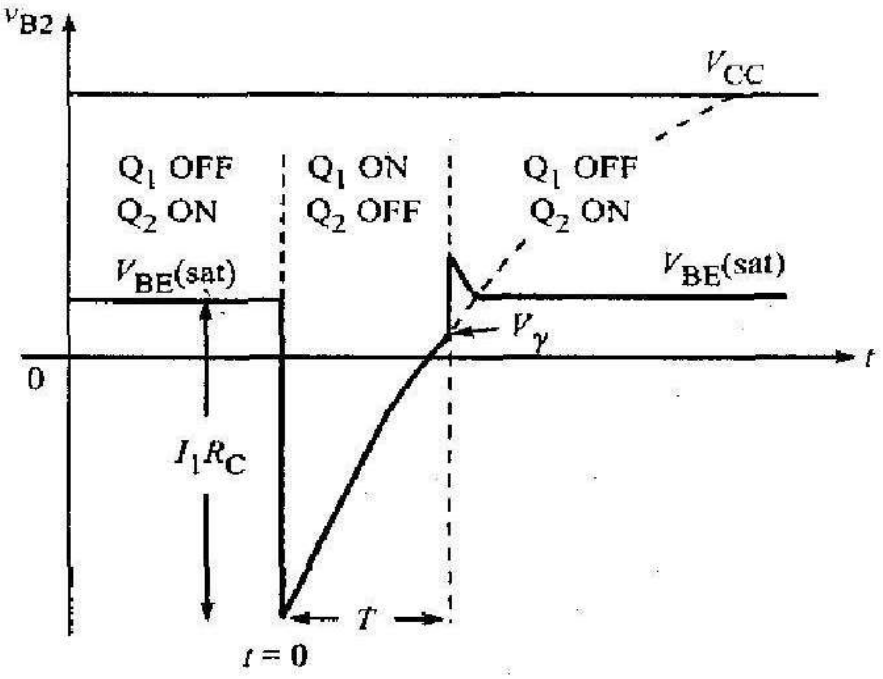


Fig a) Voltage variation at the base of Q2 during the quasi-stable state

But $I_1 R_C = V_{CC} - V_{CE}(\text{sat})$ (because at $t = 0^-$, $v_{C1} = V_{CC}$ and at $t = 0^+$, $v_{C1} = V_{CE}(\text{sat})$)

$$\therefore \quad v_{B2} = V_{CC} - [V_{CC} - \{V_{BE}(\text{sat}) - (V_{CC} - V_{CE}(\text{sat}))\}]e^{-t/\tau}$$

$$= V_{CC} - [2V_{CC} - \{V_{BE}(\text{sat}) + V_{CE}(\text{sat})\}]e^{-t/\tau}$$

At $t = T$, $v_{B2} = V_\gamma$

$$\therefore \quad V_\gamma = V_{CC} - [2V_{CC} - \{V_{CE}(\text{sat}) + V_{BE}(\text{sat})\}]e^{-T/\tau}$$

i.e. $$e^{T/\tau} = \frac{2V_{CC} - [V_{CE}(\text{sat}) + V_{BE}(\text{sat})]}{V_{CC} - V_\gamma}$$

$$\therefore \quad \frac{T}{\tau} = \frac{\ln\left[2\left(V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right)\right]}{V_{CC} - V_\gamma}$$

i.e. $$T = \tau \ln 2 + \tau \ln \frac{V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}}{V_{CC} - V_\gamma}$$

Normally for a transistor, at room temperature, the cut-in voltage is the average of the saturation junction

$$V_\gamma = \frac{V_{CE}(sat) + V_{BE}(sat)}{2}$$

voltages for either Ge or Si transistors, i.e.

Neglecting the second term in the expression for *T*

$$T = \tau \ln 2$$

$$T = (R + R_a)C \ln 2 = 0.693(R + R_a)C$$

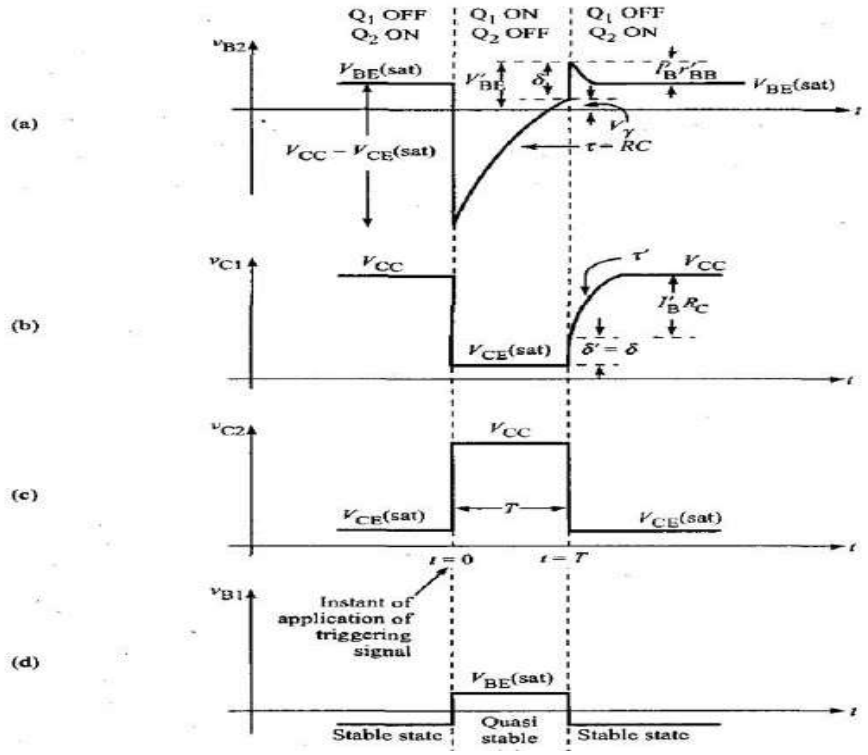
but for a transistor in saturation *Ra « R.*

Gate width, *T* = 0.693RC

The larger the *Vcc* is, compared to the saturation junction voltages, the more accura the result is. The gate width can be made very stable (almost independent of transistor characteristic supply voltages, and resistance values) if Q1 is driven into saturation during the quasi-stab state.

Waveforms of the collector-coupled monostable multivibrator

The waveforms at the collectors and bases of both the transistors Q1 and Q2 are shown below



(a) at the base of Q2, (b) at the collector of Q1, (c) at the collector of Q2, and (d) at the base of Q1

ASTABLE MULTIVIBRATOR

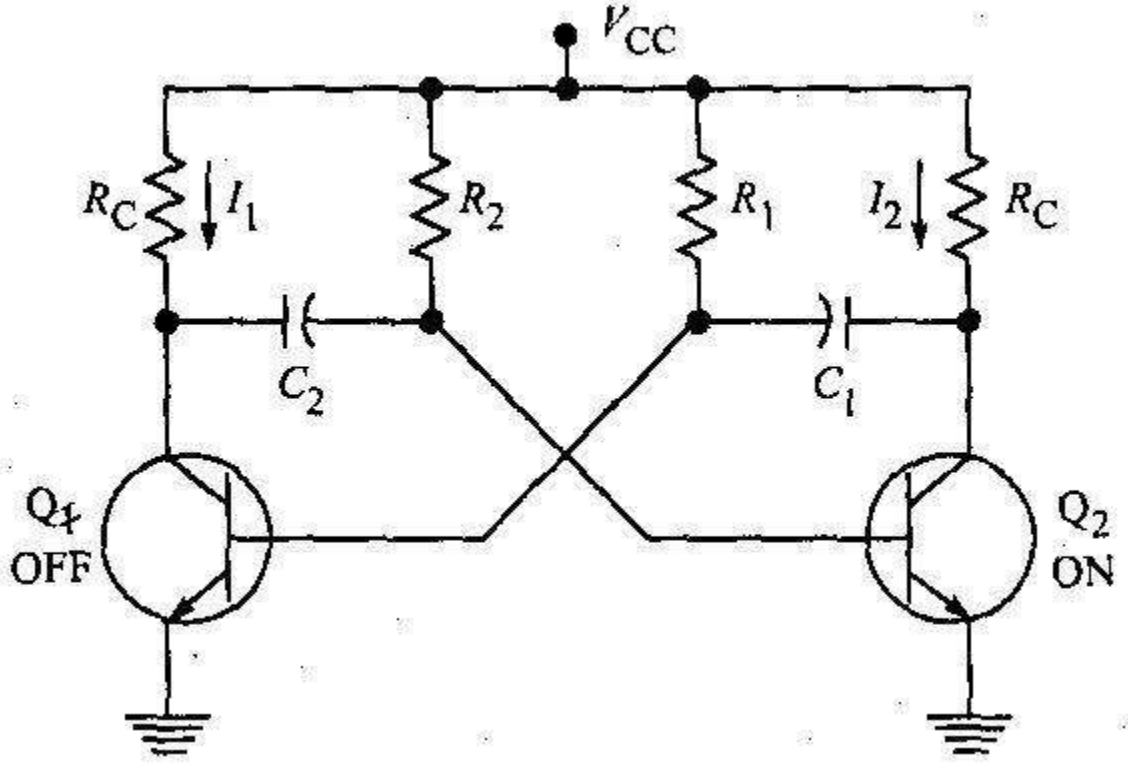
As the name indicates an astable multivibrator is a multivibrator with no permanent stable state. Both of its states are quasi stable only. It cannot remain in any one of its states indefinitely and keeps on oscillating between its two quasi stable states the moment it is connected to the supply. It remains in each of its two quasi stable states for only a short designed interval of time and then goes to the other quasi stable state. No triggering signal is required. Both the coupling elements are capacitors (ac coupling) and hence both the states are quasi stable. It is a free running multivibrator. It generates square waves. It is used as a master oscillator.

There are two types of astable multivibrators:

1. Collector-coupled astable multivibrator
2. Emitter-coupled astable multivibrator

THE COLLECTOR-COUPLED ASTABLE MULTIVIBRATOR

The below Figure shows the circuit diagram of a collector-coupled astable multivibrator using n-p-n transistors. The collectors of both the transistors Qj and Q2 are connected to the bases



of the other transistors through the coupling capacitors Cs and C2. Since both are ac couplings, neither transistor can remain permanently at cut-off. Instead, the circuit has two quasi-stable states, and it makes periodic transitions between these states. Hence it is used as a master oscillator. No triggering signal is required for this multivibrator. The component values are selected such that, the moment it is connected to the supply, due to supply transients one

transistor will go into saturation and the other into cut-off, and also due to capacitive couplings it keeps on-oscillating between its two quasi stable states.

The waveforms at the bases and collectors for the astable multivibrator, are shown in below Figure. Let us say at t = 0, Q2 goes to ON state and Q] to OFF state. So, for t < 0, Q2 was OFF and Q1 was ON

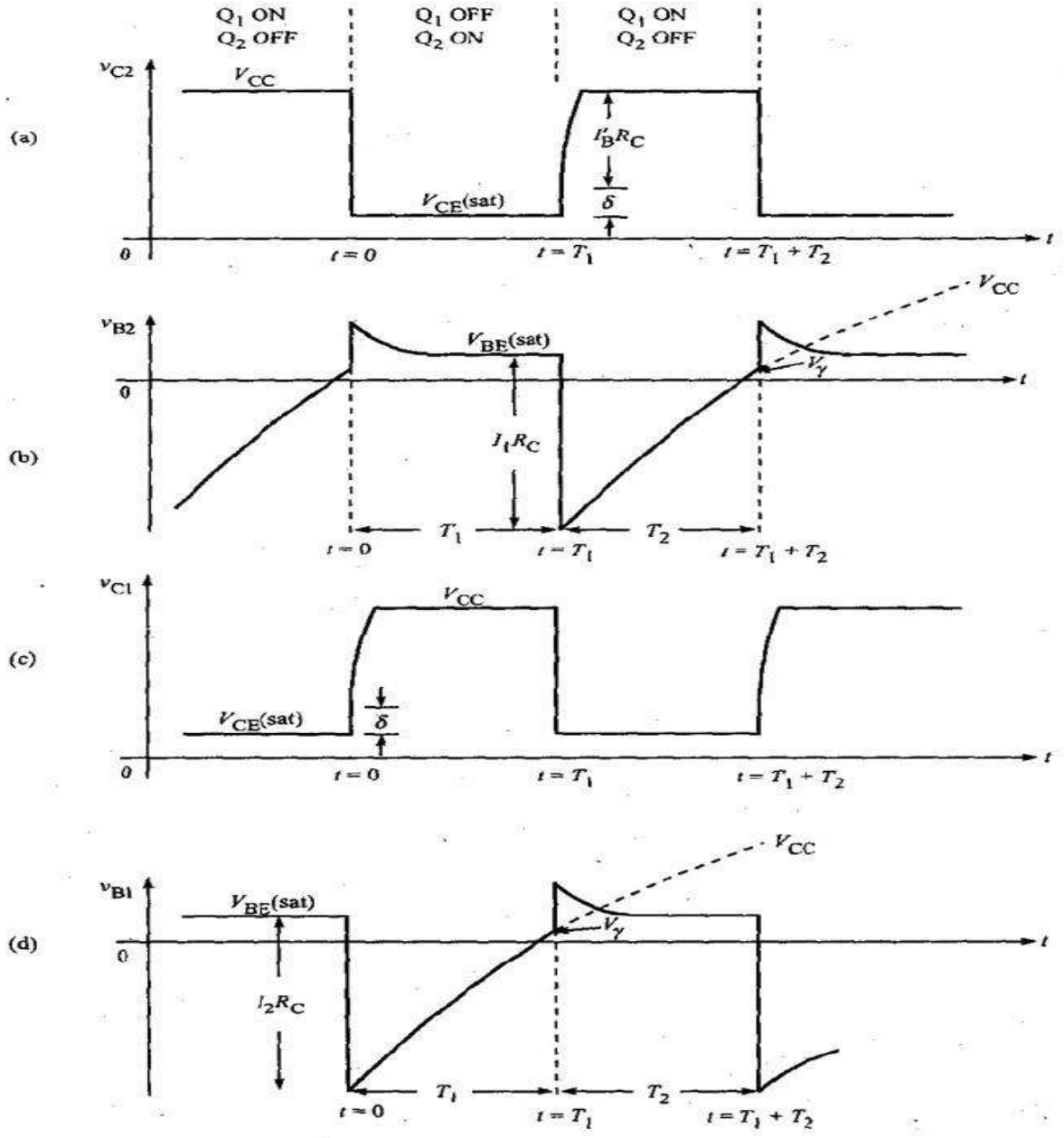


Fig: waveforms at the bases and collectors of a collector-coupled astable multivibrator

Hence for t < 0, vB2 is negative, vC2 = *Vcc,* VB! = VBE(sat) and vcj = VCE(sat). The capacitor C2 charges from Vcc through *R2* and vB2 rises exponentially towards V cc. At t = 0, vB2 reaches the cut-in voltage *Vy* and Q2 conducts. As Q2 conducts, its collector voltage Vc2 drops by /2/?c - ^cc ~ VcE(sa O- This drop in vc2 is transmitted to the base of Qj through the coupling capacitor C2

and hence vB1 also falls by /2/?c- Qi goes to OFF state. So, VB] = VBE(sat) - /2tfc, and its collector voltage vcl rises towards VCc- This rise in vc] is coupled through the coupling capacitor C2 to the base of Q2, causing an overshoot *§* in vB2 and the abrupt rise by the same amount *8* in VCL as shown in Figure 4.51(c). Now since Q2 is ON, *C*\ charges from *Vcc* through *Rlt* and hence VB] rises exponentially. At *t* = 7"], when VB! rises to *VY,* Qi conducts and due to regenerative action Qi goes into saturation and Q2 to cut-off. Now, for *t > T*\, the coupling capacitor C2 charges from Vcc through *R2* and at / = 7", + 7"2, when vB2 rises to the cut-in voltage Vr, Q2 conducts and due to regenerative feedback Q2 goes to ON state and Q| to OFF state. The cycle of events repeats and the circuit keeps on oscillating between its two quasi-stable states. Hence the output is a square wave. It is called a square wave generator or square wave oscillator or relaxation oscillator. It is a free running oscillator.

Expression for the frequency of oscillation of an astable multivibrator

Consider the waveform at the base of Q_1 shown in Figure 4.54(d). At $t = 0$,

$$v_{B1} = V_{BE}(\text{sat}) - I_2R_C$$

But
$$I_2R_C = V_{CC} - V_{CE}(\text{sat})$$

$\therefore$ At $t = 0$, $v_{B1} = V_{BE}(\text{sat}) - V_{CC} + V_{CE}(\text{sat})$

For $0 < t < T_1$, v_{B1} rises exponentially towards V_{CC} given by the equation,

$$v_o = v_f - (v_f - v_i)e^{-t/\tau}$$

$\therefore$ $v_{B1} = V_{CC} - [V_{CC} - (V_{BE}(\text{sat}) - V_{CC} + V_{CE}(\text{sat}))]e^{-t/\tau_1}$, where $\tau_1 = R_1C_1$

At $t = T_1$, when v_{B1} rises to V_γ, Q_1 conducts

$\therefore$ $$V_\gamma = V_{CC} - [2V_{CC} - (V_{BE}(\text{sat}) + V_{CE}(\text{sat}))]e^{-T_1/R_1C_1}$$

or
$$e^{T_1/R_1C_1} = \frac{2\left[V_{CC} - \dfrac{V_{BE}(\text{sat}) + V_{CE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln \frac{2\left[V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

$$T_1 = R_1C_1 \ln 2 + R_1C_1 \ln \frac{\left[V_{CC} - \dfrac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}\right]}{V_{CC} - V_\gamma}$$

At room temperature for a transistor,

$$V_\gamma \simeq \frac{V_{CE}(\text{sat}) + V_{BE}(\text{sat})}{2}$$

$\therefore$ $$T_1 = R_1C_1 \ln 2 = 0.693R_1C_1$$

On similar lines considering the waveform of above Figure , we can show that the time *T2* for which Q2 is OFF and Q1 is ON is given by The period of the waveform, The frequency of oscillation, If *R{ = R2 = R,* and Cs = C2 = C, then TI = *T2* = T.

$$T = 2 \times 0.693RC = 1.386RC \qquad \text{and} \qquad f = \frac{1}{1.386RC}$$

The frequency of oscillation may be varied over the range from cycles to mega cycles by varying *RC.* It is also possible to vary the frequency electrically by connecting *R1* and *R2* to an auxiliary voltage source *V* (the collector supply remains +VCC) and then varying this voltage *V.*

THE EMITTER-COUPLED ASTABLE MULTIVIBRATOR

An emitter-coupled astable multivibrator may be obtained by using three power supplies or a single power supply. The below Figure (a) shows the circuit diagram of a free-running emitter coupled multivibrator using n-p-n transistors. Figure 4.64 shows its waveforms. Three power supplies are indicated for the sake of simplifying the analysis. A more practical circuit using a single supply is indicated in below Figure (b). Let us assume that the circuit operates in such a manner that Q1 switches between cut-off and saturation and Q2 switches between cut-off and its active region.

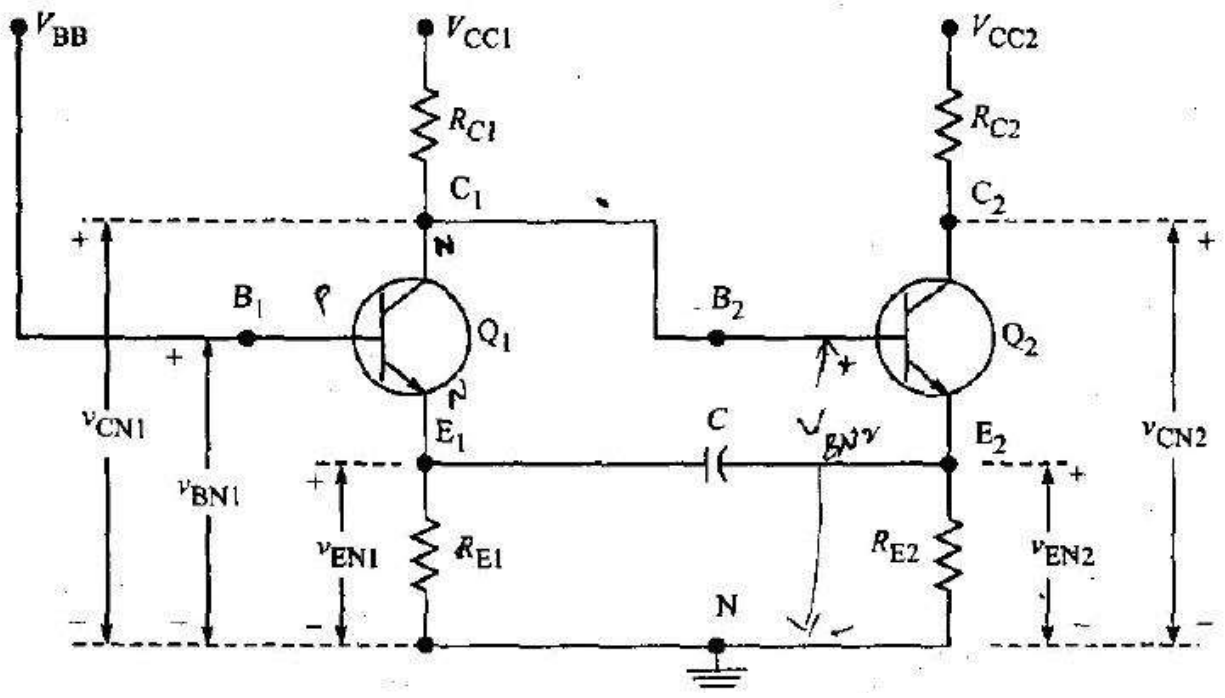


Fig a) Astable Emitter-Coupled Multivibrator

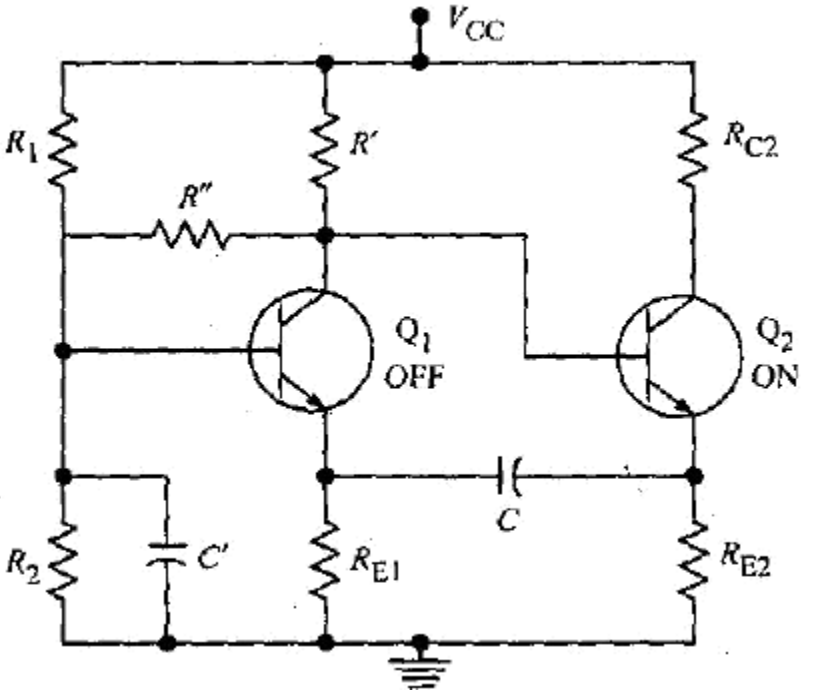


Fig b) Emitter Coupled multivibrator

The waveforms at the base and collector are as shown below:

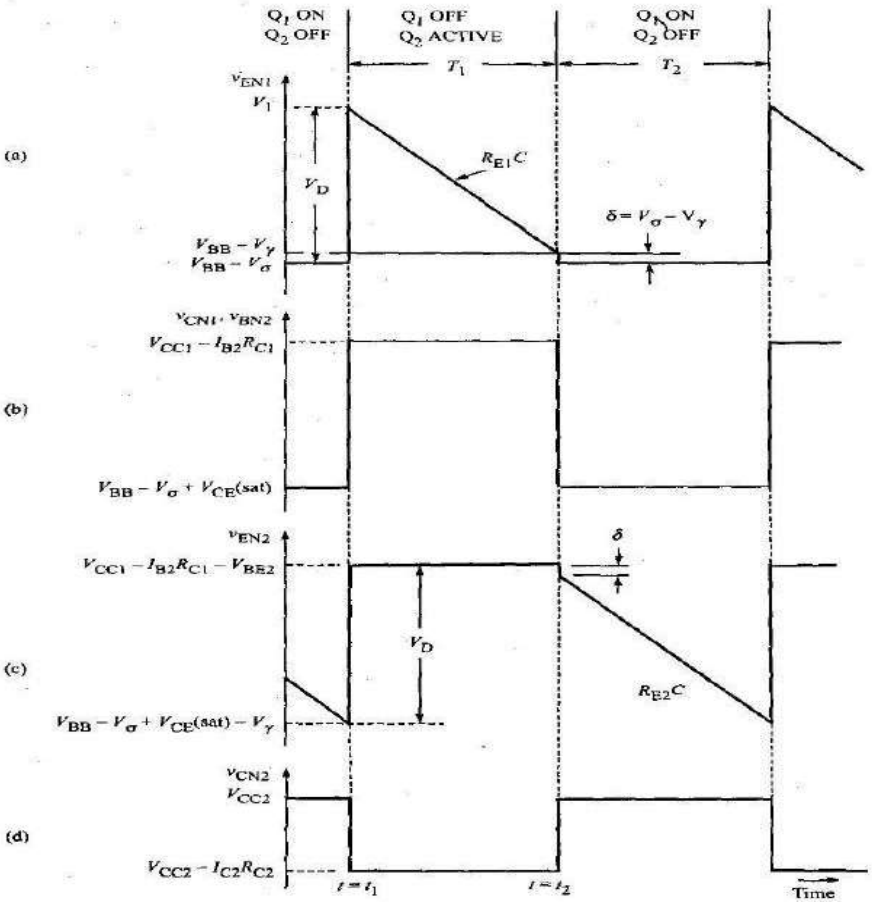


Fig waveforms of the emitter-coupled astable multivibrator

Advantages

1. It is inherently self-starting.
2. The collector of Q2 where the output is taken may be loaded heavily even capacitively.
3. The output is free of recovery transients.
4. Because it has an isolated input at the base of Q1, synchronization is convenient.
5. Frequency adjustment is convenient because only one capacitor is used.

Disadvantages

1. This circuit is more difficult to adjust for proper operating conditions.
2. This circuit cannot be operated with *T1* and T2 widely different.
3. This circuit uses more components than does the collector-coupled circuit.